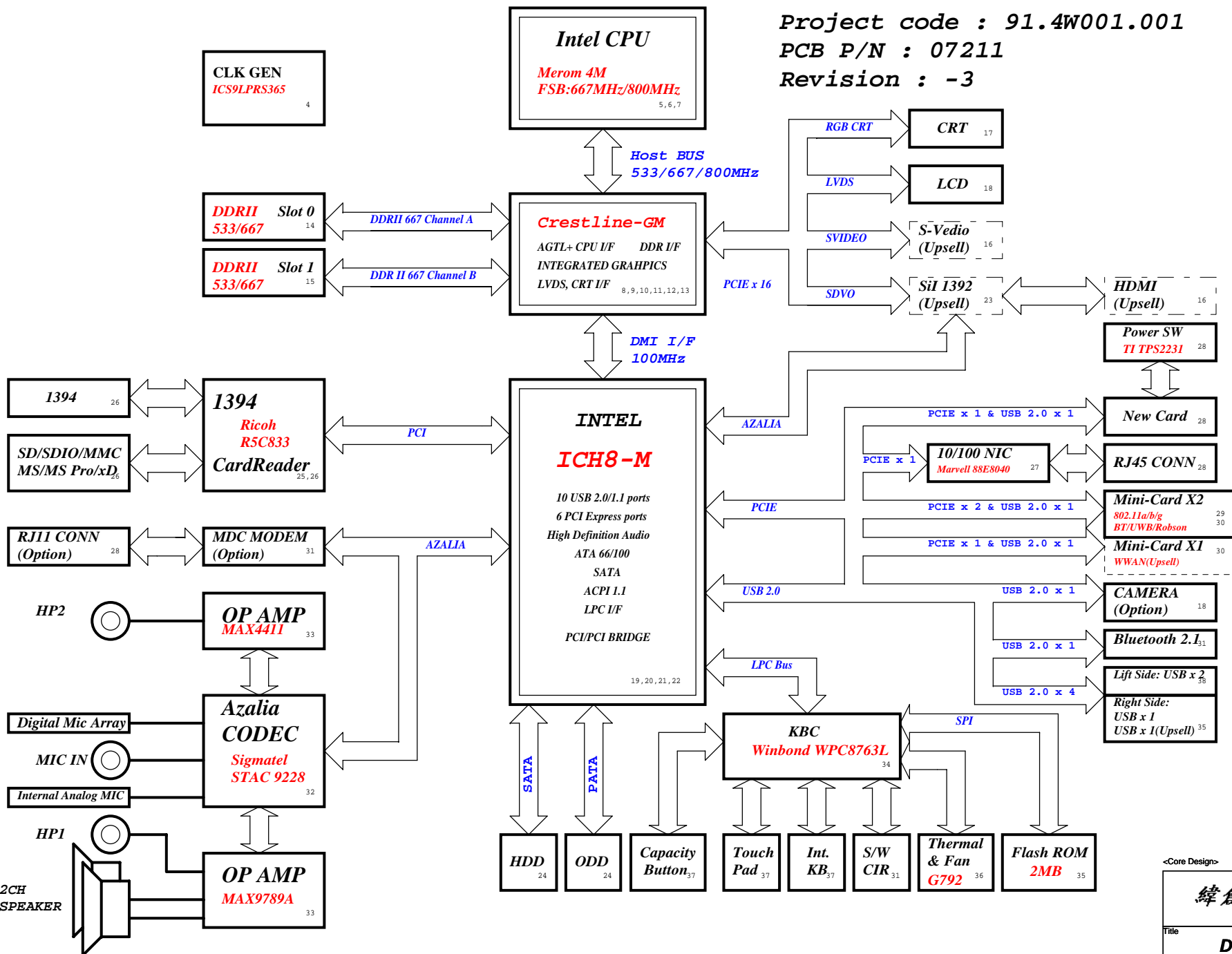


Spears Intel UMA Block Diagram 2008/01/14

Project code : 91.4W001.001

PCB P/N : 07211

Revision : -3



CPU DC/DC	
ISL6262A 41, 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC	
TPS5117 43, 44	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
	1D8V_S3

SYSTEM DC/DC	
TPS51120 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5
	3D3V_AUX_S5
	5V_S5
	3D3V_S5

SYSTEM DC/DC	
TPS51100 45	
INPUTS	OUTPUTS
1D8V_S3	DDR_VREF_S0
	DDR_VREF_S3

SYSTEM DC/DC	
LDO 45	
INPUTS	OUTPUTS
3D3V_S0	2D5V_S0
1D8V_S3	1D5V_S0
1D8V_S4	1D25V_S0

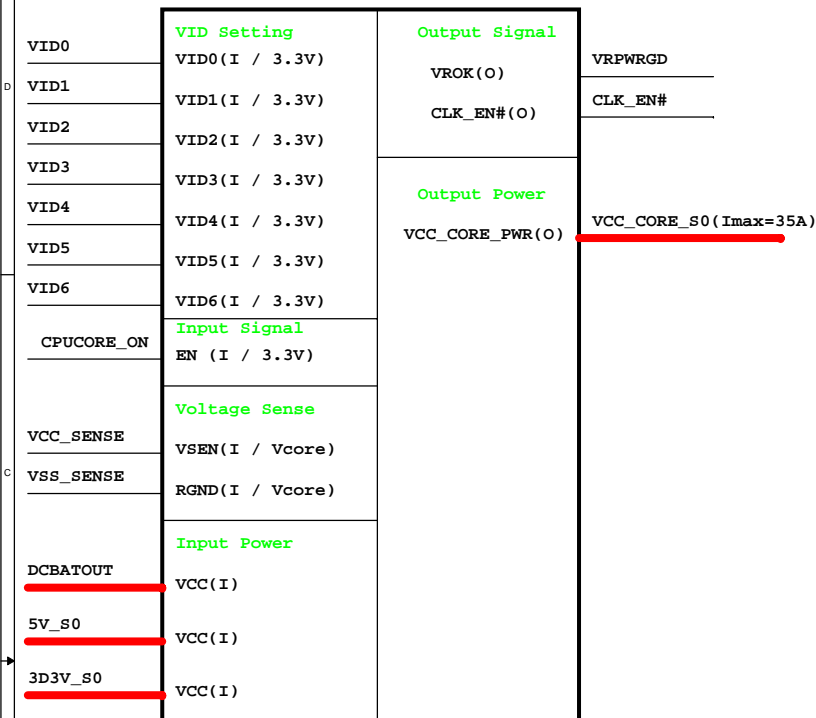
MAXIM CHARGER	
MAX8731A 39	
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	

<Core Design>

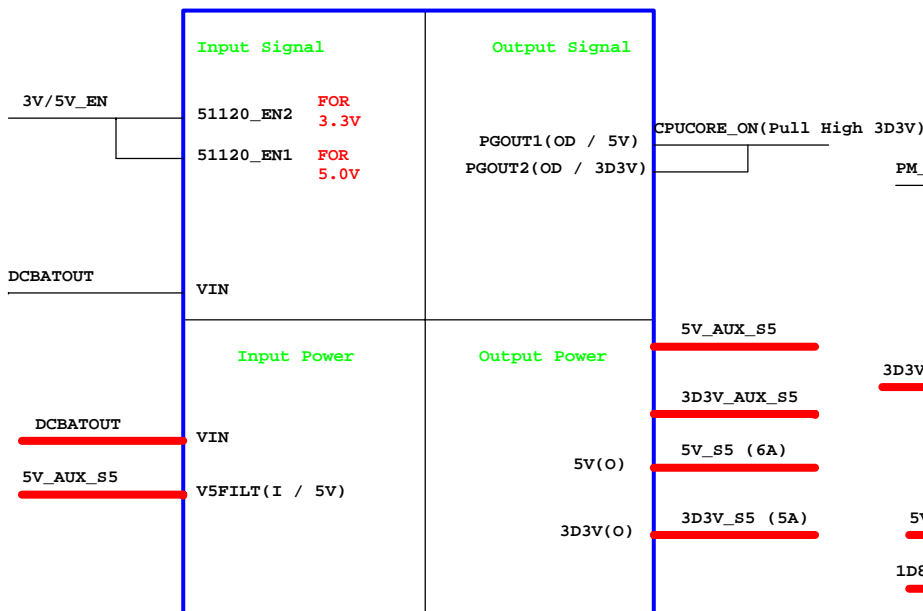
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DS2 System Block Diagram			
Size	Document Number	Rev	
A3	Spears-Intel	-3	
Date:	Monday, January 21, 2008	Sheet 1 of 47	

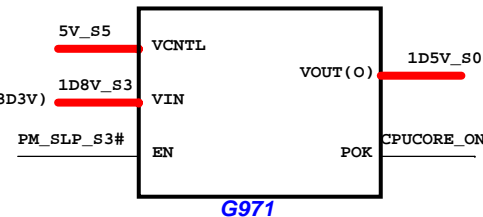
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ISL6262A



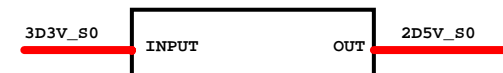
TI TPS51120
3D3V/5V



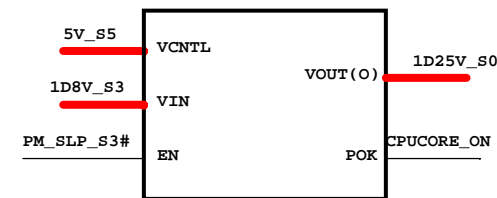
1D5V_S0



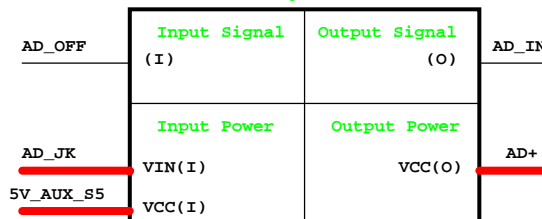
2D5V_S0



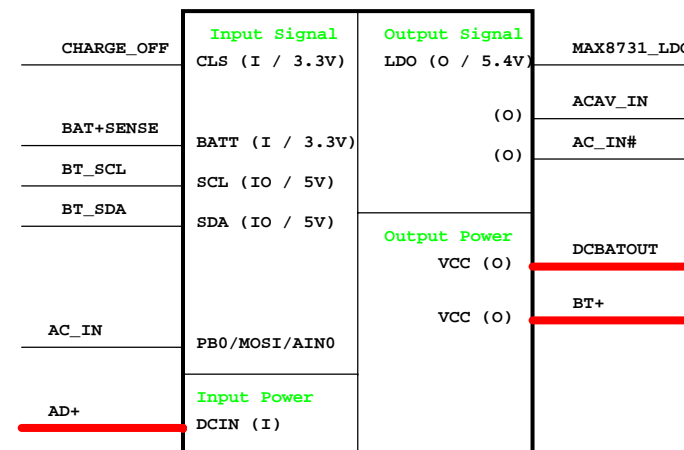
G9131
1D25V_S0



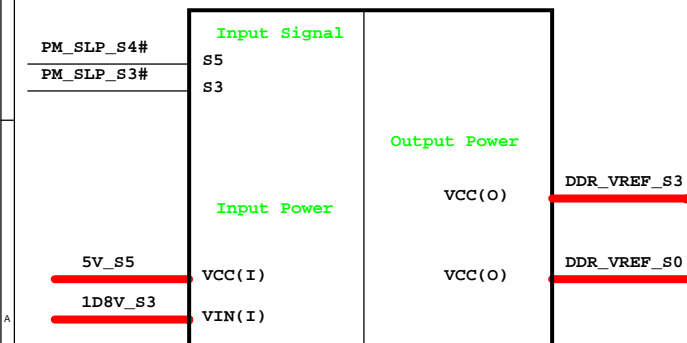
Adapter



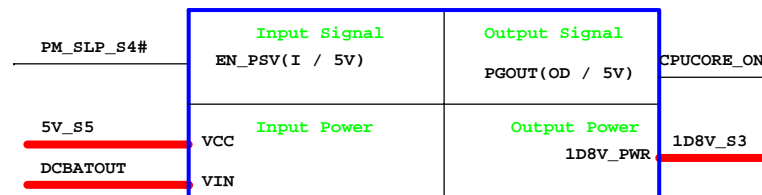
Charger_MAX8731A



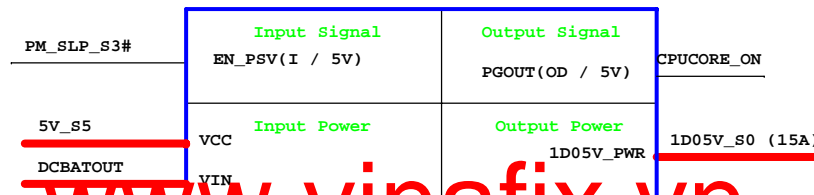
TI TPS51100
0.9V/DDR_VREF_S3



TPS51117_1D8V_S3



TPS51117_1D05V



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Title
Size A3
Document Number
Date: Monday, January 21, 2008
Sheet 2 of 47
Rev -3

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVP3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCT_GNT3#	low = A16 swap override enable high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable Low=Disable	
Integrated VccLAN1_05VccCL1_05		
LAN100_SLP	High=Enable Low=Disable	

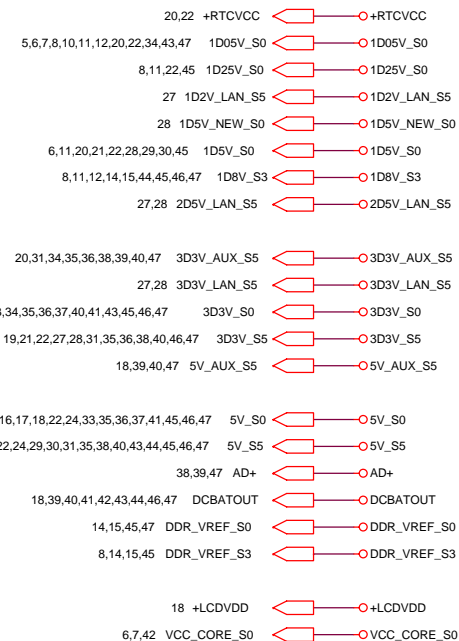
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



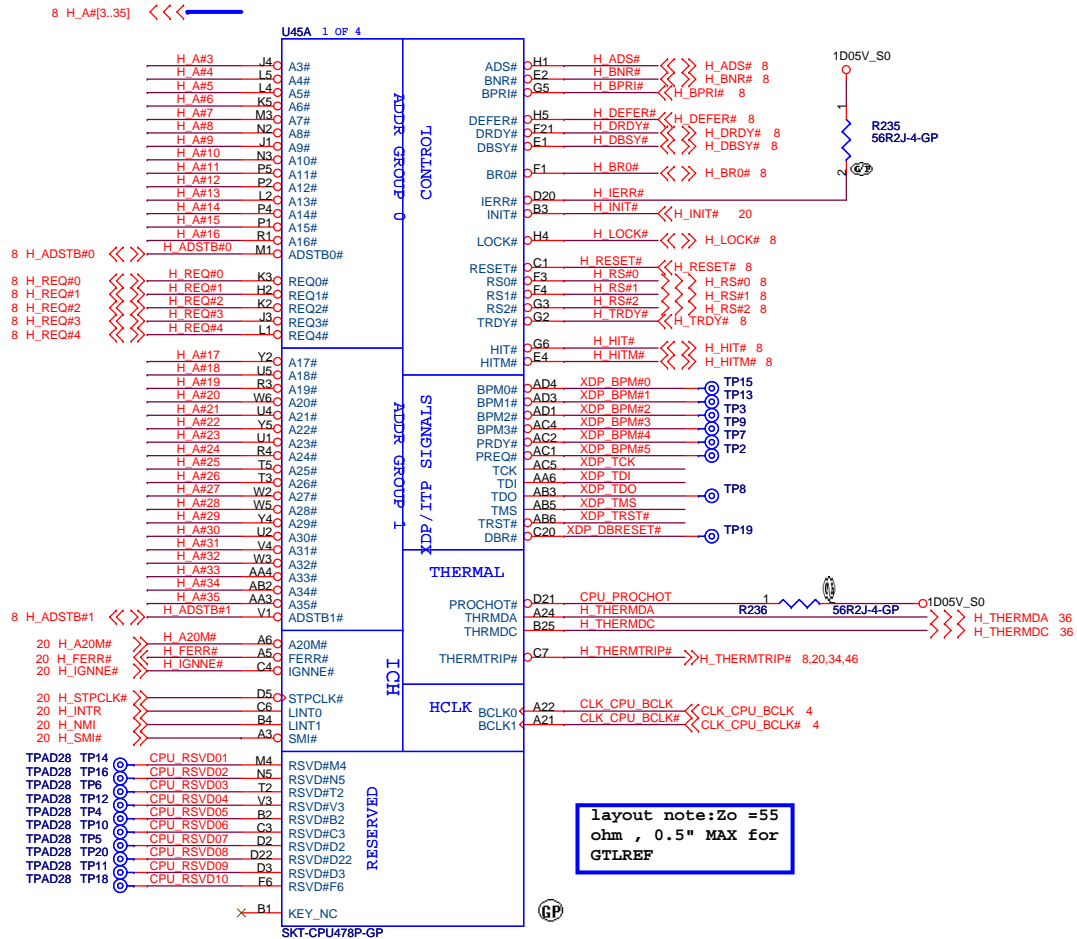
INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present
CFG 12 CFG 13 LL(0)	XOR/ALL-Z	Reserved
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	

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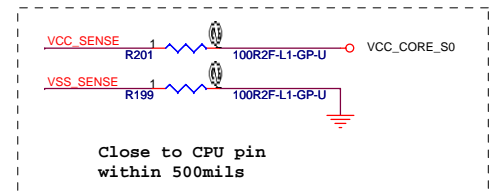
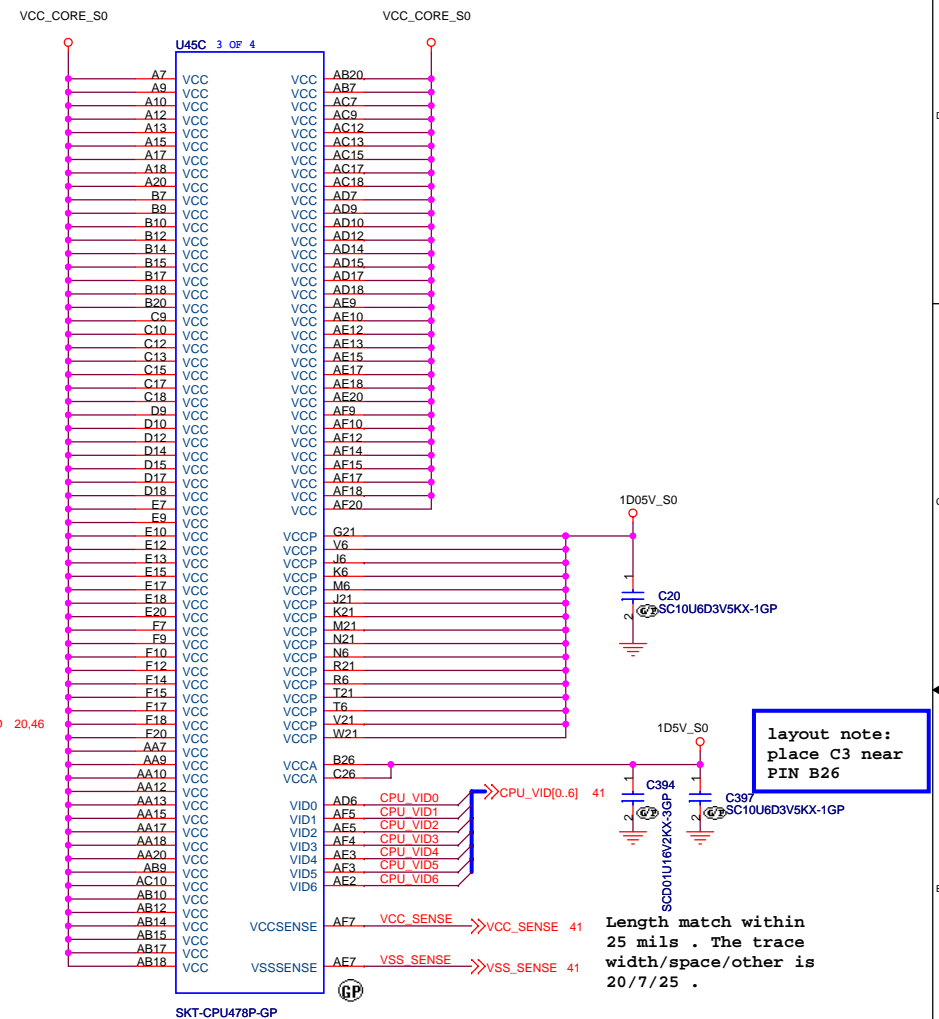
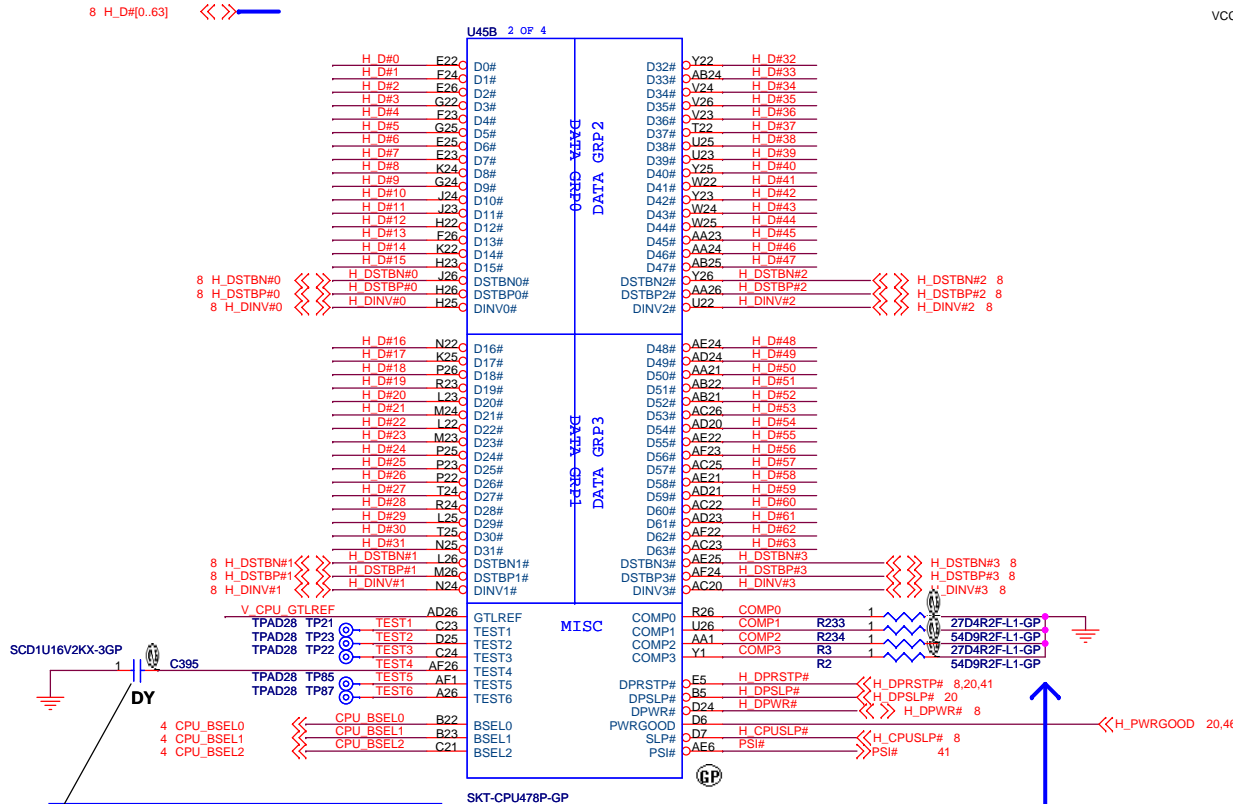
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Title	DS2-Intel	Rev -3
Size A3	Document Number	
Date: Monday, January 21, 2008	Sheet 3 of 47	

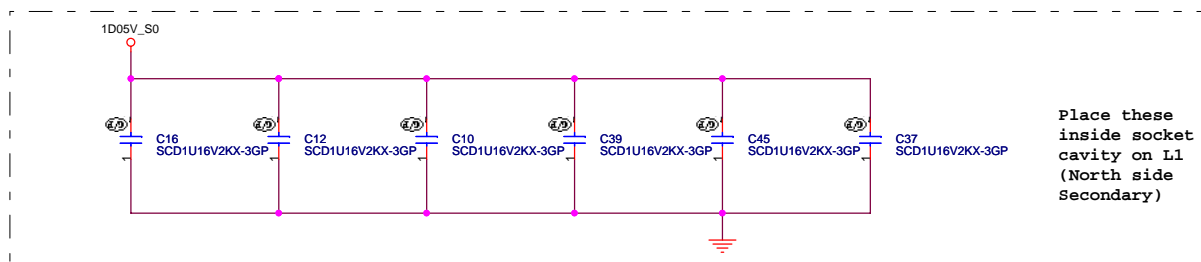
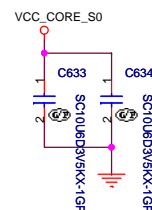
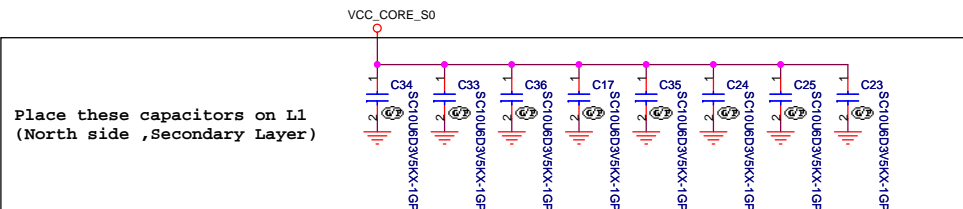
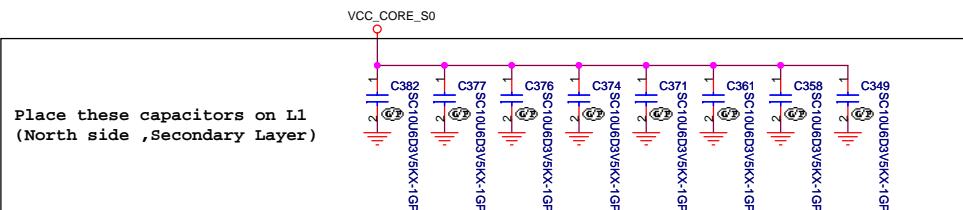
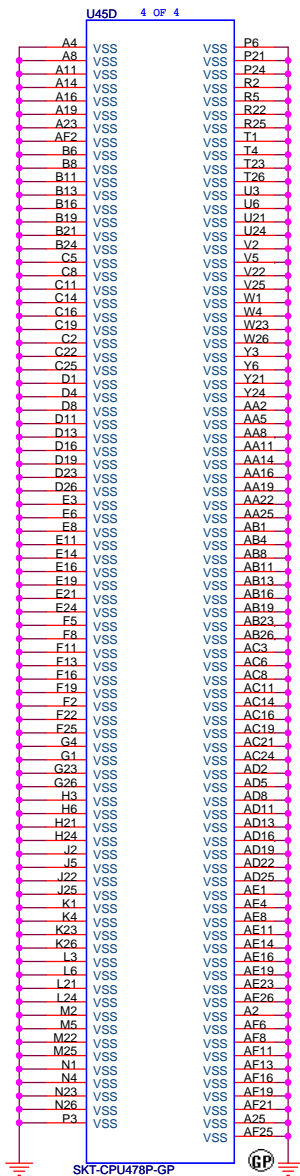


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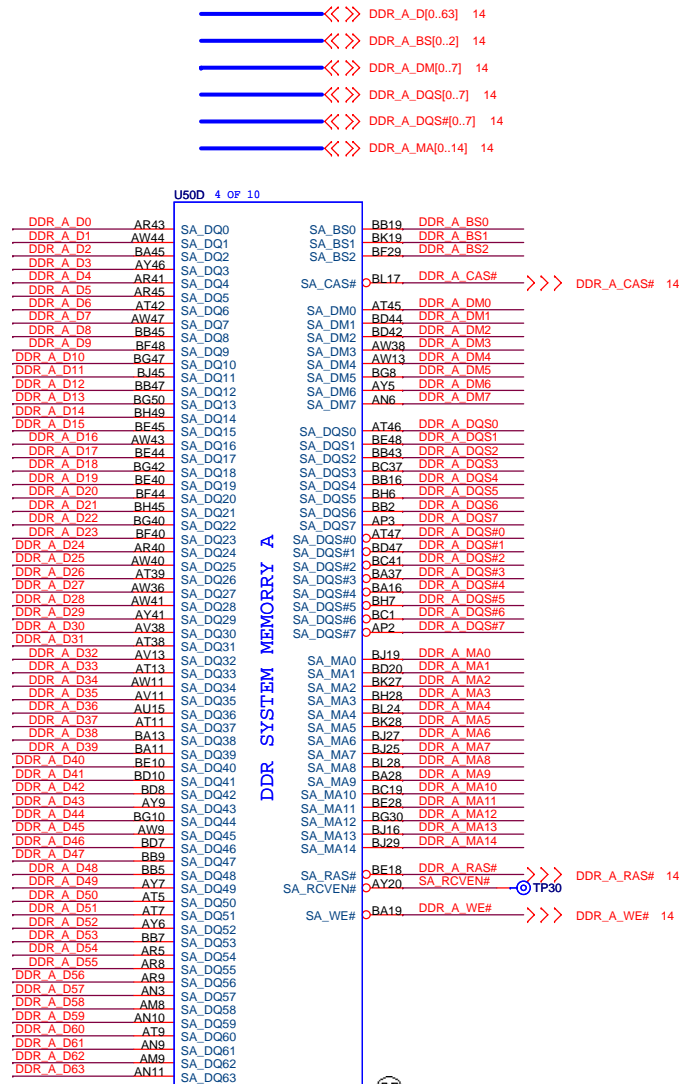
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Merom(1/3)-AGTL+/XDP		
Size	Document Number	Rev
A3	DS2-Intel	-3
Date:	Monday, January 21, 2008	Sheet 5 of 47

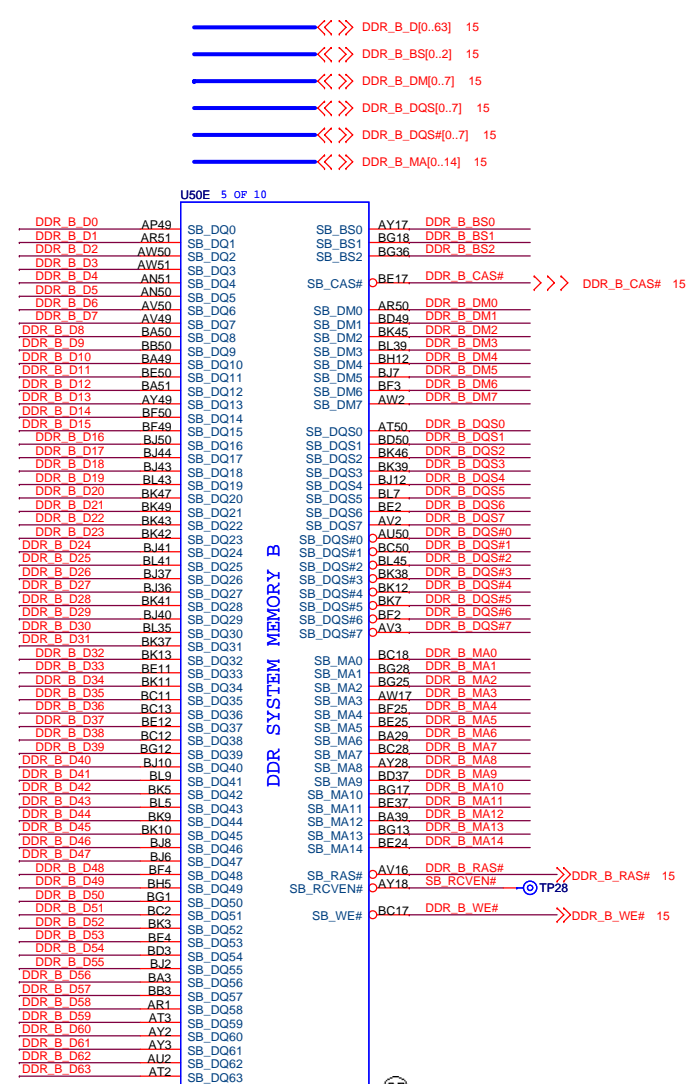








NB:71.GM965.A0U

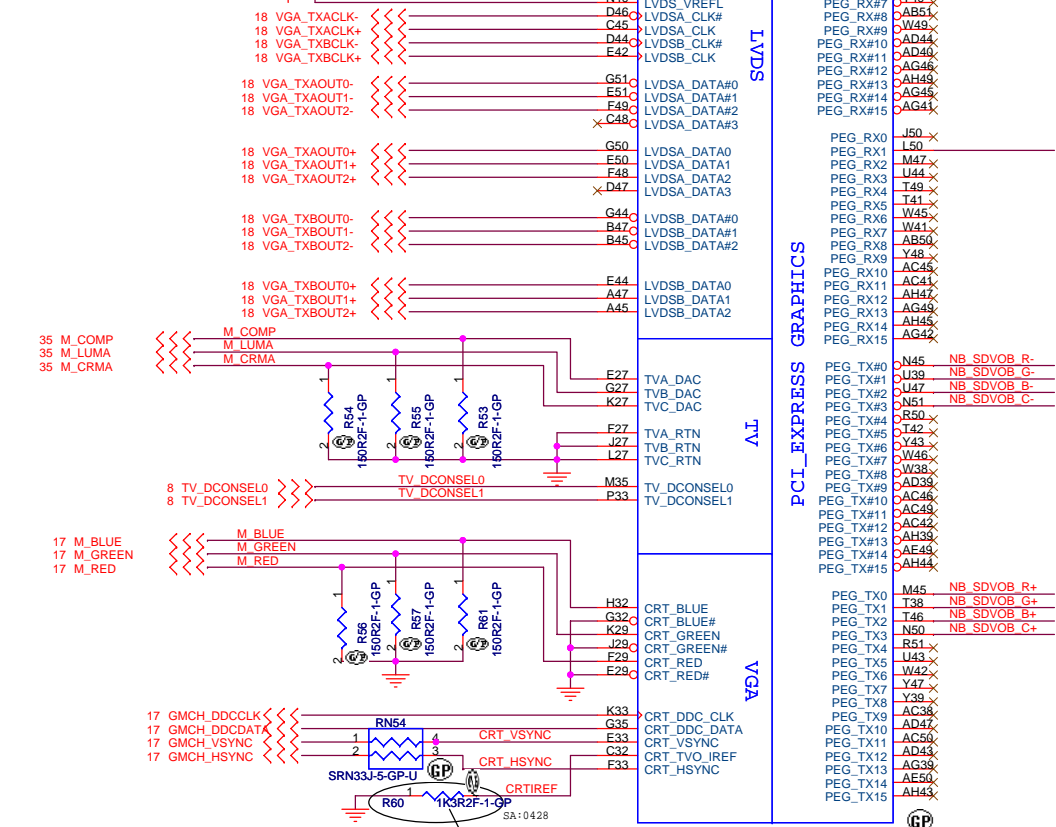


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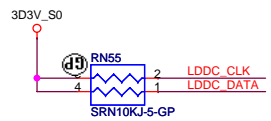
For Crestline : 2.4 Kohm
For Calero : 1.5Kohm

-1.0908 Chang R68 from
64.24015.6DL to 64.33015.6DL



FOR Calero: 255 ohm
Crestline: 1.3k ohm

NB:71.GM965.A0U



1D05V_S0
R74 240R2F-L-GP
PEGCOMP trace width and spacing is 20/25 mils.

Strap Pin Table

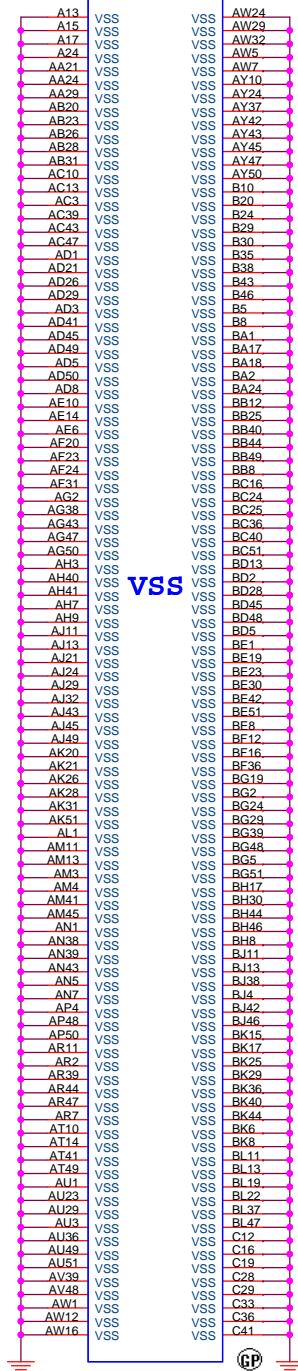
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.





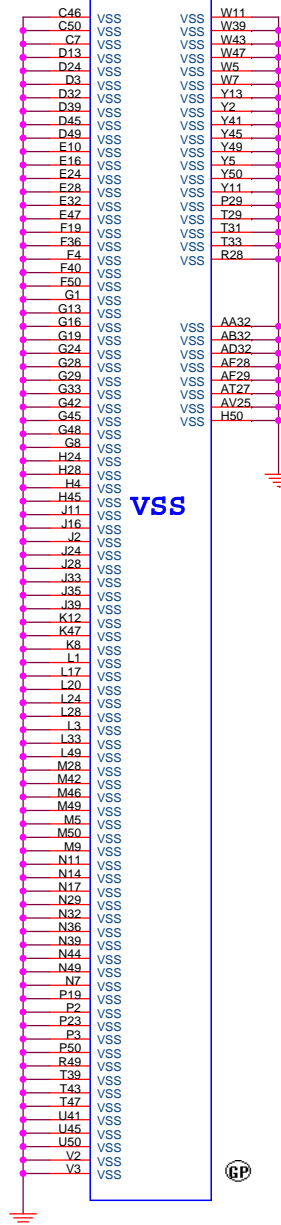


U50I 9 OF 10



NB: 71.GM965.A0U

U50J10 OF 10

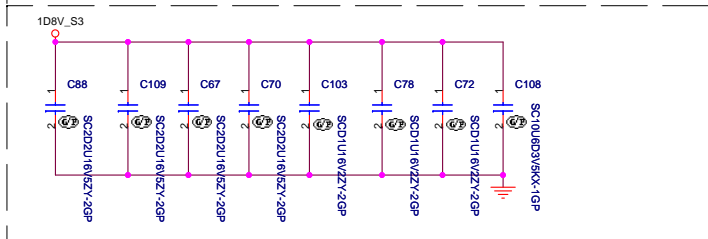


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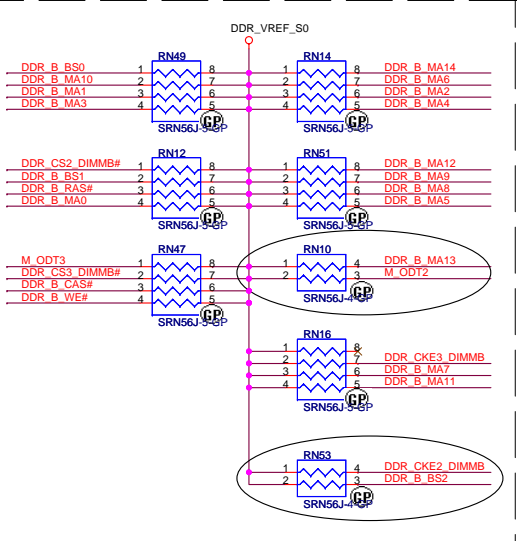
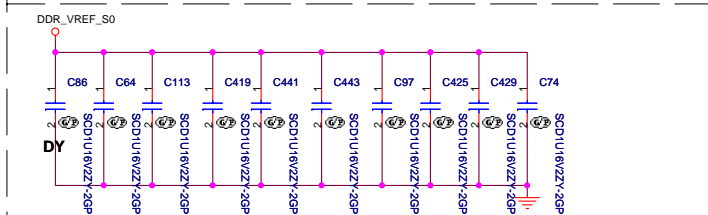
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Title	
CRESTLINE(6/6)-PWR/GND	
Size	Document Number
A3	DS2-Intel
Date: Monday, January 21, 2008	Sheet 13 of 47
Rev	
-3	

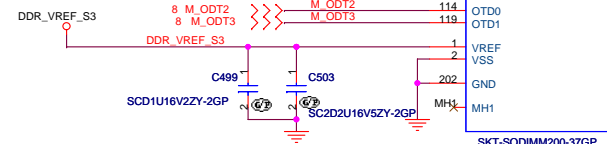
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors closely DM2, all trace length Max=1.5"



DDR_B_MA0	102	A0	108	DDR_B_RAS#	<<>>	DDR_B_RAS# 9
DDR_B_MA1	101	A1	109	DDR_B_WE#	<<>>	DDR_B_WE# 9
DDR_B_MA2	100	A2	113	DDR_B_CAS#	<<>>	DDR_B_CAS# 9
DDR_B_MA3	99	A3	110	DDR_CS2_DIMMB#	<<>>	DDR_CS2_DIMMB# 8
DDR_B_MA4	98	A4	115	DDR_CS3_DIMMB#	<<>>	DDR_CS3_DIMMB# 8
DDR_B_MA5	97	A5	79	DDR_CKE2_DIMMB	<<>>	DDR_CKE2_DIMMB 8
DDR_B_MA6	96	A6	80	DDR_CKE3_DIMMB	<<>>	DDR_CKE3_DIMMB 8
DDR_B_MA7	95	A7	30	M_CLK_DDR2	<<>>	M_CLK_DDR2 8
DDR_B_MA8	94	A8	32	M_CLK_DDR3	<<>>	M_CLK_DDR3 8
DDR_B_MA9	93	A9	164	M_CLK_DDR3	<<>>	M_CLK_DDR3 8
DDR_B_MA10	92	A10/AP	166	M_CLK_DDR3	<<>>	M_CLK_DDR3 8
DDR_B_MA11	91	A11	10	DDR_B_DM0	<<>>	DDR_B_DM0 8
DDR_B_MA12	90	A12	26	DDR_B_DM1	<<>>	DDR_B_DM1 8
DDR_B_MA13	89	A13	52	DDR_B_DM2	<<>>	DDR_B_DM2 8
DDR_B_MA14	88	A14	67	DDR_B_DM3	<<>>	DDR_B_DM3 8
DDR_B_MA15	87	A15	130	DDR_B_DM4	<<>>	DDR_B_DM4 8
DDR_B_MA16	86	A16/BA2	147	DDR_B_DM5	<<>>	DDR_B_DM5 8
DDR_B_MA17	85	BA0	170	DDR_B_DM6	<<>>	DDR_B_DM6 8
DDR_B_MA18	84	BA1	185	DDR_B_DM7	<<>>	DDR_B_DM7 8
DDR_B_MA19	83	DO0	195	ICH_SMBDATA	<<>>	ICH_SMBDATA 4.14,21
DDR_B_MA20	82	DO1	197	ICH_SMBCLK	<<>>	ICH_SMBCLK 4.14,21
DDR_B_MA21	81	DO2	199	VDDSPD	<<>>	VDDSPD
DDR_B_MA22	80	DO3	198	R36	<<>>	R36
DDR_B_MA23	79	DO4	200	R38	<<>>	R38
DDR_B_MA24	78	DO5	50	NC#50	<<>>	NC#50
DDR_B_MA25	77	DO6	69	NC#69	<<>>	NC#69
DDR_B_MA26	76	DO7	83	NC#83	<<>>	NC#83
DDR_B_MA27	75	DO8	120	NC#120	<<>>	NC#120
DDR_B_MA28	74	DO9	163	NC#163/TEST	<<>>	NC#163/TEST
DDR_B_MA29	73	DO10	81	VDD	<<>>	VDD
DDR_B_MA30	72	DO11	82	VDD	<<>>	VDD
DDR_B_MA31	71	DO12	87	VDD	<<>>	VDD
DDR_B_MA32	70	DO13	88	VDD	<<>>	VDD
DDR_B_MA33	69	DO14	95	VDD	<<>>	VDD
DDR_B_MA34	68	DO15	96	VDD	<<>>	VDD
DDR_B_MA35	67	DO16	103	VDD	<<>>	VDD
DDR_B_MA36	66	DO17	104	VDD	<<>>	VDD
DDR_B_MA37	65	DO18	111	VDD	<<>>	VDD
DDR_B_MA38	64	DO19	112	VDD	<<>>	VDD
DDR_B_MA39	63	DO20	117	VDD	<<>>	VDD
DDR_B_MA40	62	DO21	118	VDD	<<>>	VDD
DDR_B_MA41	61	DO22	3	VSS	<<>>	VSS
DDR_B_MA42	60	DO23	8	VSS	<<>>	VSS
DDR_B_MA43	59	DO24	9	VSS	<<>>	VSS
DDR_B_MA44	58	DO25	12	VSS	<<>>	VSS
DDR_B_MA45	57	DO26	15	VSS	<<>>	VSS
DDR_B_MA46	56	DO27	18	VSS	<<>>	VSS
DDR_B_MA47	55	DO28	21	VSS	<<>>	VSS
DDR_B_MA48	54	DO29	24	VSS	<<>>	VSS
DDR_B_MA49	53	DO30	25	VSS	<<>>	VSS
DDR_B_MA50	52	DO31	28	VSS	<<>>	VSS
DDR_B_MA51	51	DO32	33	VSS	<<>>	VSS
DDR_B_MA52	50	DO33	34	VSS	<<>>	VSS
DDR_B_MA53	49	DO34	35	VSS	<<>>	VSS
DDR_B_MA54	48	DO35	40	VSS	<<>>	VSS
DDR_B_MA55	47	DO36	41	VSS	<<>>	VSS
DDR_B_MA56	46	DO37	42	VSS	<<>>	VSS
DDR_B_MA57	45	DO38	47	VSS	<<>>	VSS
DDR_B_MA58	44	DO39	48	VSS	<<>>	VSS
DDR_B_MA59	43	DO40	53	VSS	<<>>	VSS
DDR_B_MA60	42	DO41	54	VSS	<<>>	VSS
DDR_B_MA61	41	DO42	59	VSS	<<>>	VSS
DDR_B_MA62	40	DO43	60	VSS	<<>>	VSS
DDR_B_MA63	39	DO44	65	VSS	<<>>	VSS
DDR_B_MA64	38	DO45	66	VSS	<<>>	VSS
DDR_B_MA65	37	DO46	71	VSS	<<>>	VSS
DDR_B_MA66	36	DO47	72	VSS	<<>>	VSS
DDR_B_MA67	35	DO48	77	VSS	<<>>	VSS
DDR_B_MA68	34	DO49	78	VSS	<<>>	VSS
DDR_B_MA69	33	DO50	121	VSS	<<>>	VSS
DDR_B_MA70	32	DO51	122	VSS	<<>>	VSS
DDR_B_MA71	31	DO52	127	VSS	<<>>	VSS
DDR_B_MA72	30	DO53	128	VSS	<<>>	VSS
DDR_B_MA73	29	DO54	132	VSS	<<>>	VSS
DDR_B_MA74	28	DO55	133	VSS	<<>>	VSS
DDR_B_MA75	27	DO56	138	VSS	<<>>	VSS
DDR_B_MA76	26	DO57	139	VSS	<<>>	VSS
DDR_B_MA77	25	DO58	144	VSS	<<>>	VSS
DDR_B_MA78	24	DO59	145	VSS	<<>>	VSS
DDR_B_MA79	23	DO60	149	VSS	<<>>	VSS
DDR_B_MA80	22	DO61	150	VSS	<<>>	VSS
DDR_B_MA81	21	DO62	155	VSS	<<>>	VSS
DDR_B_MA82	20	DO63	156	VSS	<<>>	VSS
DDR_B_MA83	19	DO64	161	VSS	<<>>	VSS
DDR_B_MA84	18	DO65	162	VSS	<<>>	VSS
DDR_B_MA85	17	DO66	165	VSS	<<>>	VSS
DDR_B_MA86	16	DO67	168	VSS	<<>>	VSS
DDR_B_MA87	15	DO68	171	VSS	<<>>	VSS
DDR_B_MA88	14	DO69	172	VSS	<<>>	VSS
DDR_B_MA89	13	DO70	177	VSS	<<>>	VSS
DDR_B_MA90	12	DO71	178	VSS	<<>>	VSS
DDR_B_MA91	11	DO72	183	VSS	<<>>	VSS
DDR_B_MA92	10	DO73	184	VSS	<<>>	VSS
DDR_B_MA93	9	DO74	187	VSS	<<>>	VSS
DDR_B_MA94	8	DO75	190	VSS	<<>>	VSS
DDR_B_MA95	7	DO76	193	VSS	<<>>	VSS
DDR_B_MA96	6	DO77	196	VSS	<<>>	VSS
DDR_B_MA97	5	DO78	201	VSS	<<>>	VSS
DDR_B_MA98	4	DO79	MH2	VSS	<<>>	VSS
DDR_B_MA99	3	DO80	MH1	VSS	<<>>	VSS
DDR_B_MA100	2	DO81	GND	VSS	<<>>	VSS

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File

DDR2-SODIMM SLOT2

Size

Document Number

DS2-Intel

Rev

-3

Date

Monday, January 21, 2008

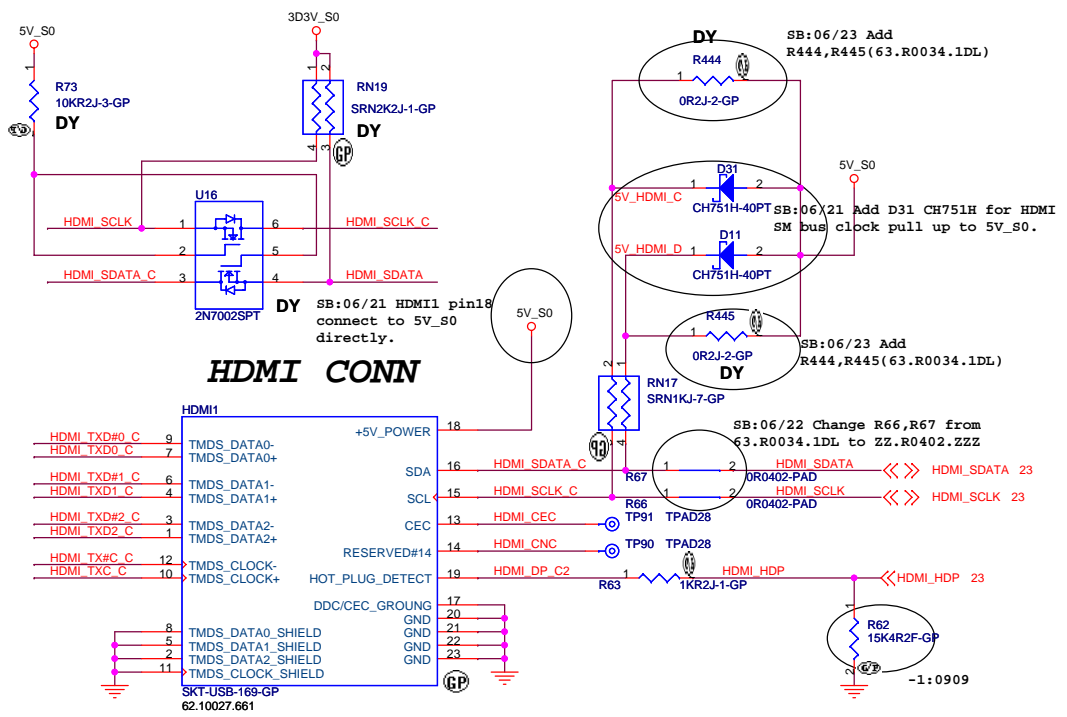
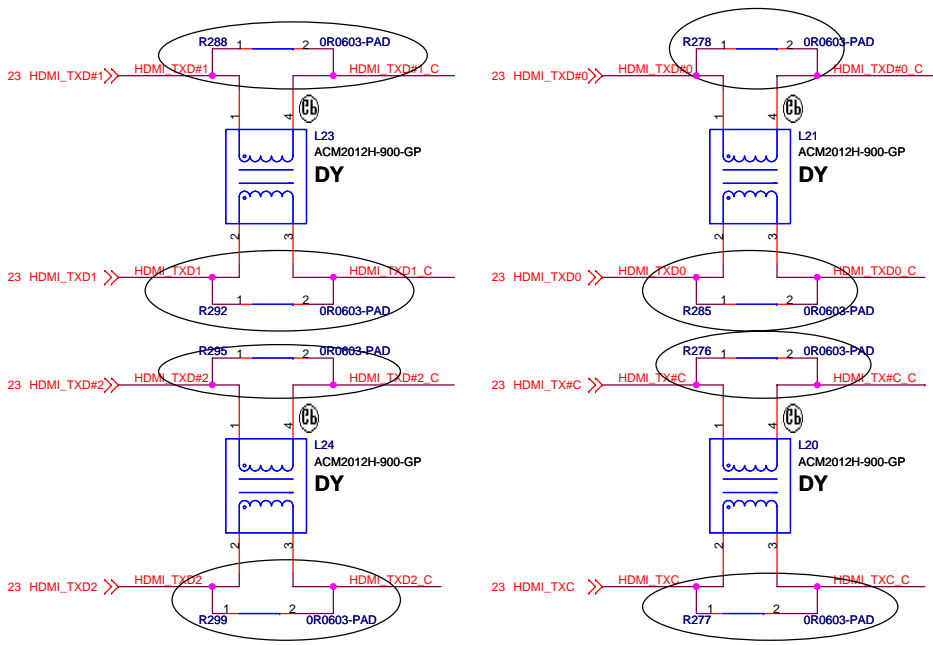
Sheet

15

of

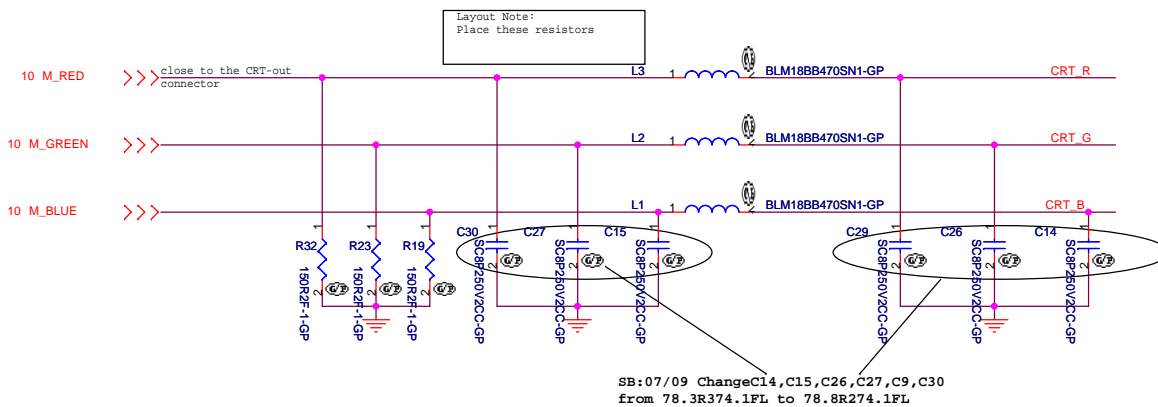
47

HDMI I/F & CONNECTOR

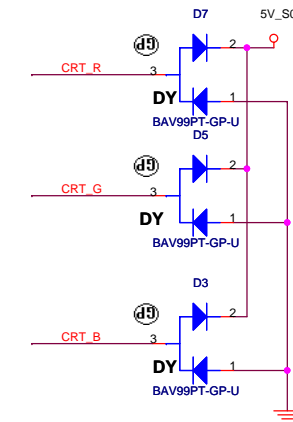
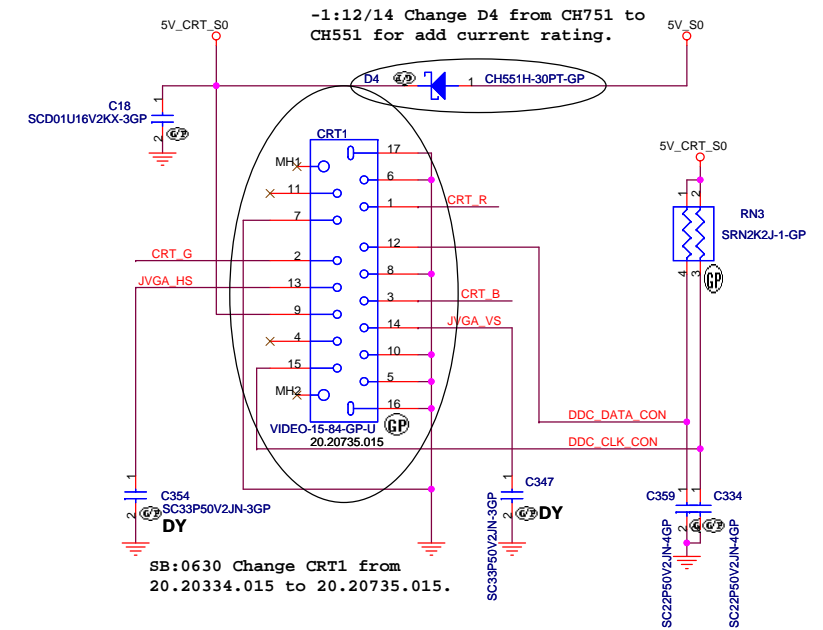
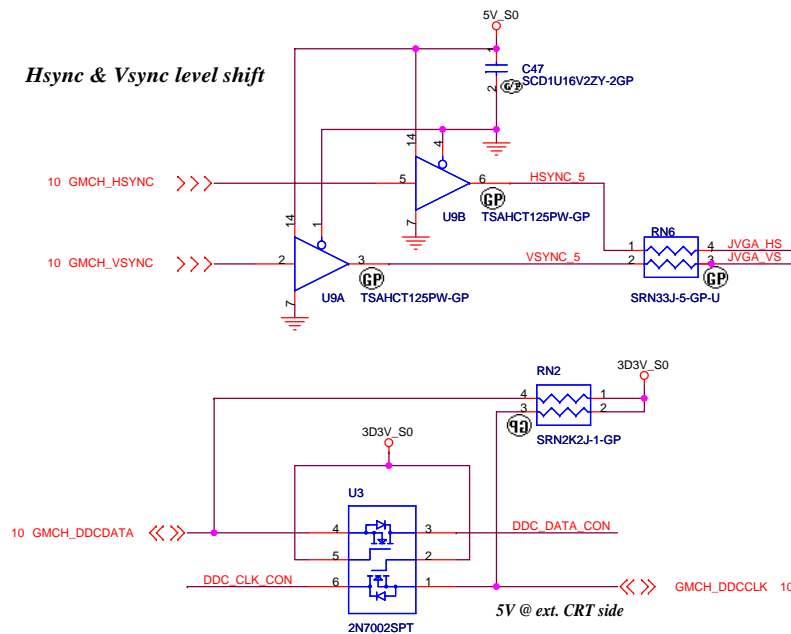


TV OUT CONN (Optional) Move to Right I/O Board

CRT I/F & CONNECTOR



Hsync & Vsync level shift



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size A3	Document Number DS2-Intel	Rev -3
Date: Monday, January 21, 2008	Sheet 17 of 47	

Diagram illustrating the LCD TST circuit. The circuit includes a capacitor labeled EC60 (3P50V2.JN-3GP) connected to the LCD TST line and ground. Another capacitor labeled EC161 (3P50V2.JN-3GP) is connected to the 5V_AUX S5 line and ground. The components are labeled DY and EC60/EC161.

SC:08/09 Add
EC161(78.10491.4FL)
for EMI request
.Default is DUMMY

SC:08/13 Add
EC167,EC168(78.10034.1FL),
R460,R461(63.R0034.1DL) place
cross LVDS CLK A,Bpair.
Default is DY.This is for RF
request.

-1:08/29 Change
LVDS channel A and
channel B EMI
solution. this is
for antena team
request.

SC:08/13 Add
EC169,EC170,EC171,
R462,R463,R464 on
LVDS channel A each
data pairs. This is
for RF request
.Default is DY.

SC:08/09 Add
EC151(78.22124.2FL)
for EMI request
.Default is DUMMY

SC:08/09 Add
EC152(78.22124.2FL)
for EMI request
.Default is DUMMY

-1:09/11

S0

V_AUD_DMIC

R189
0R0603-PAD

100MHz

0.5ohm DC

EC154

C341

EC156

DY

SCDUI6/ZZ-20P

SC4DU6D3/3KX-GF

GC:08/09 Add
SCI514(78.10491.4FL)
for EMI request
Default is DUMMY




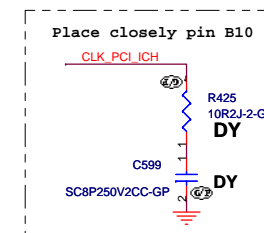
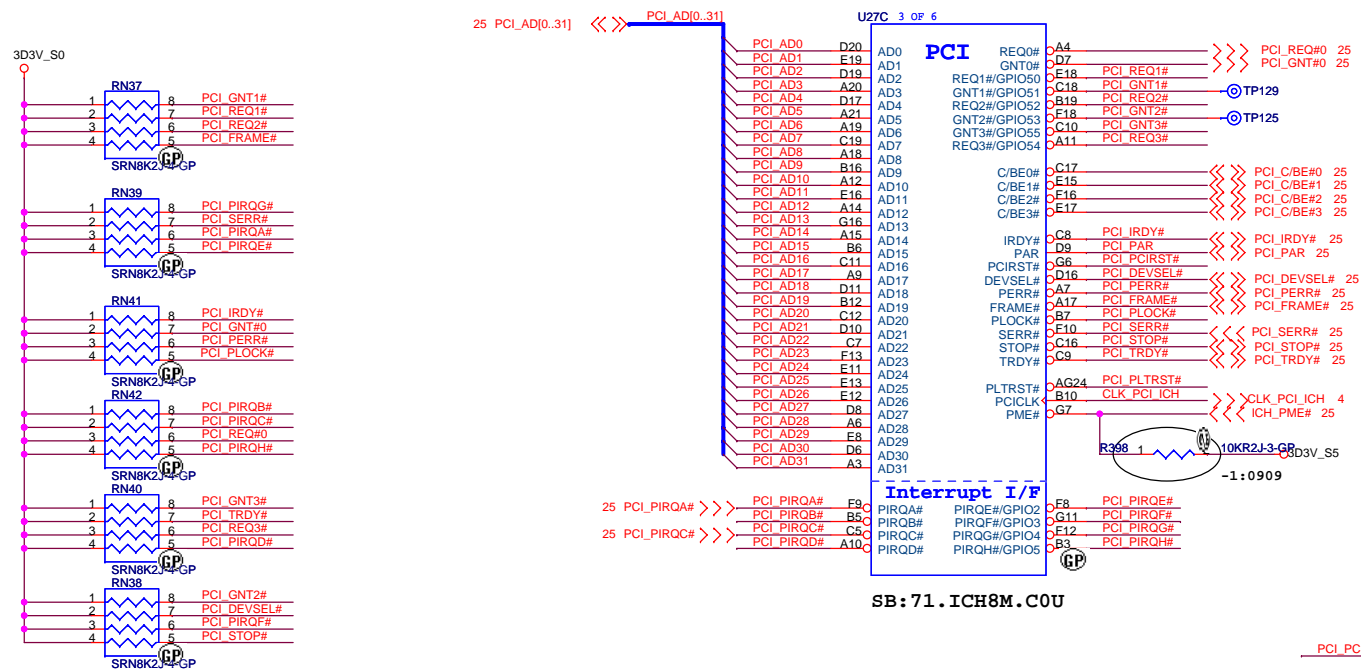
Diagram showing the pin connections for the CAMERA1 connector. The pins are numbered 1 through 10. Pin 1 is connected to +5V_RUN_CAMERA. Pin 2 is connected to AUD DMIC CLK G_R. Pin 3 is connected to AUD DMIC INO_R. Pin 4 is connected to CAMERA USB1-. Pin 5 is connected to CAMERA USB1+. Pin 6 is connected to CAMERA USB1+. Pin 7 is connected to CAMERA USB1+. Pin 8 is connected to CAMERA USB1+. Pin 9 is connected to CAMERA USB1+. Pin 10 is connected to MLX-1-GP-U.

SC:08/09 Add ~~ECI~~56(78.33034.1FL)
for EMI request .Default is DUMMY

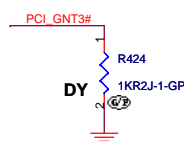
SC:08/09 Add EC155(78.33034.1EL)
for EMI request .Default is DUMMY

-1:09/11

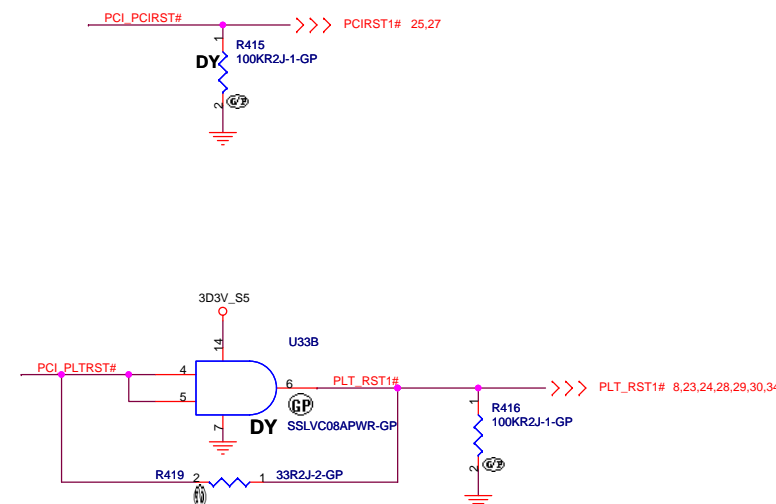
[illegible]



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



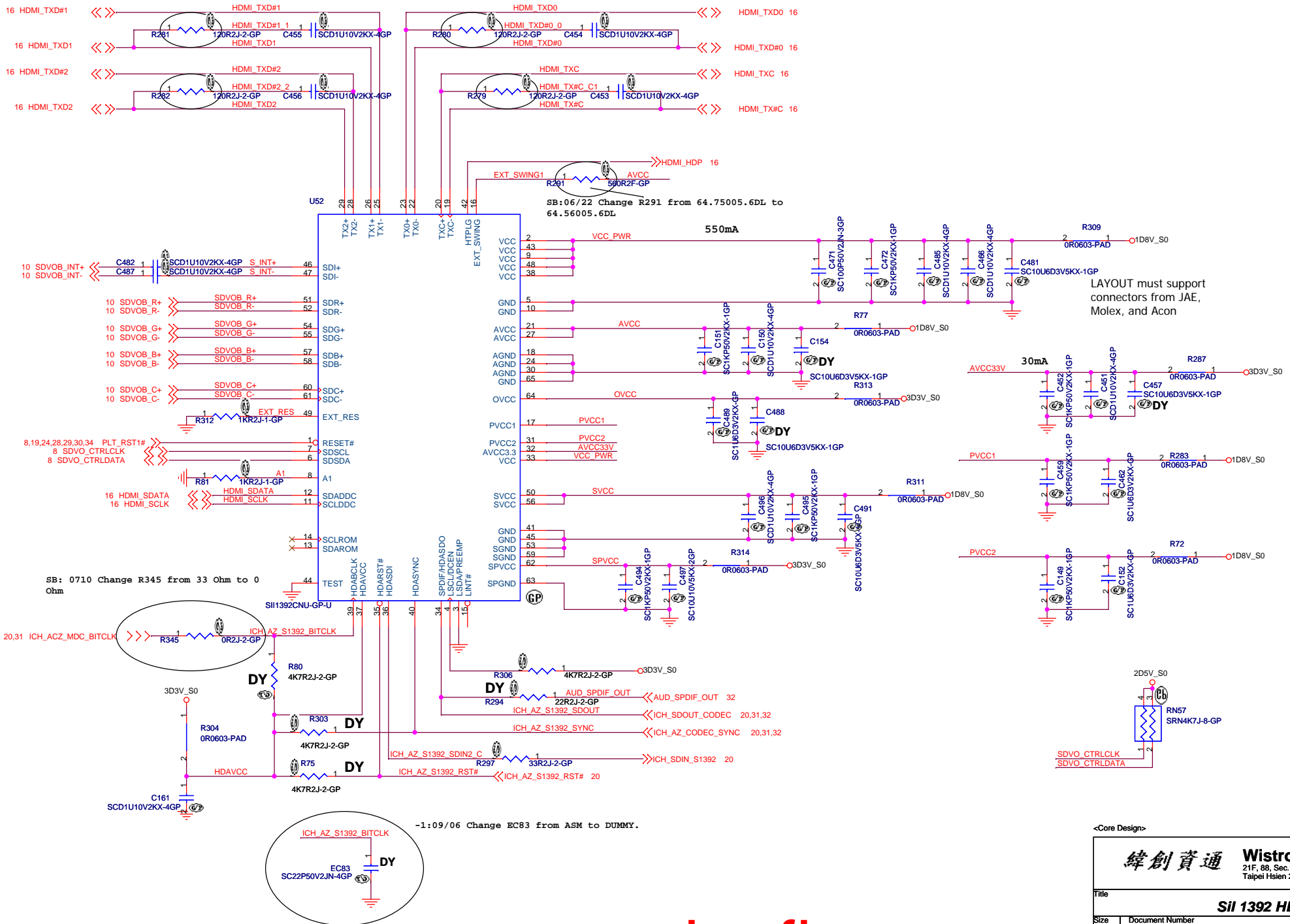
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *







SB:06/22 Change R279,R280,R281,R282 from 63.30134.1DL
to 63.12134.1DL



<Core Design>

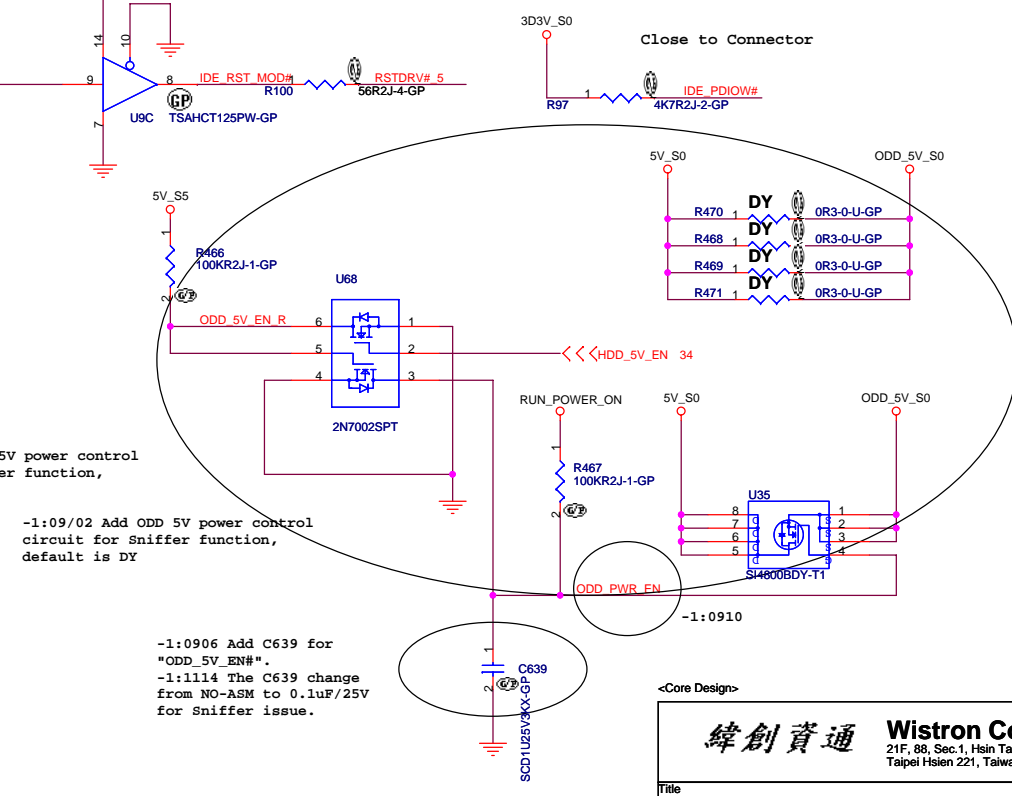
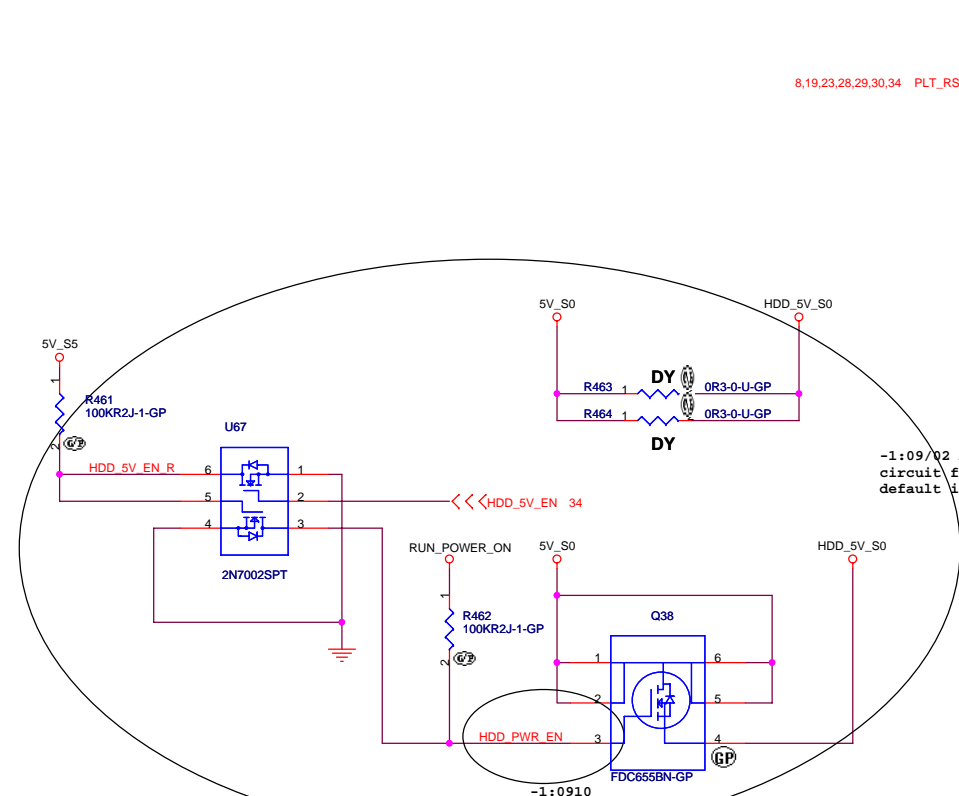
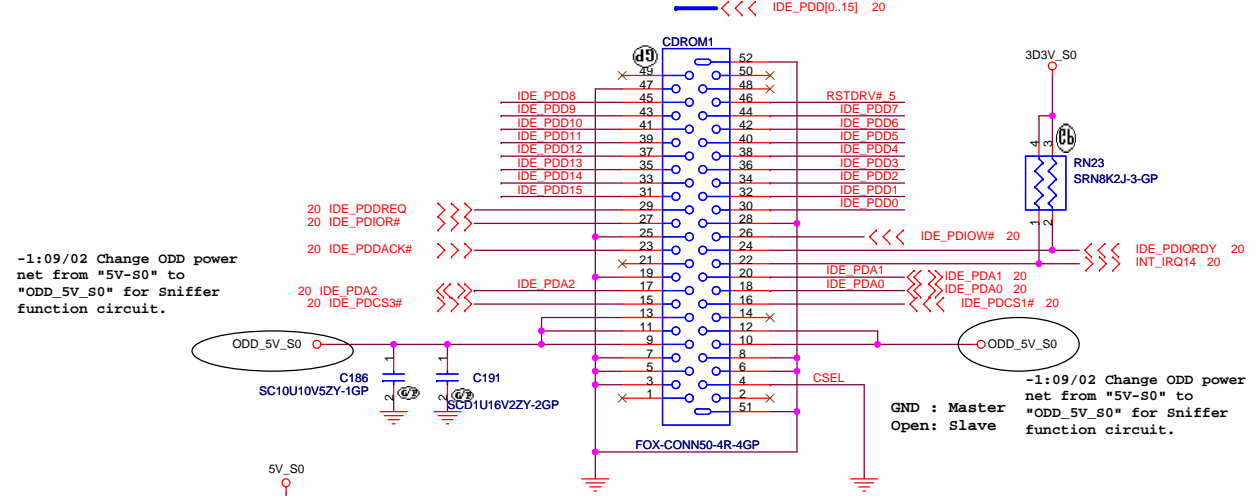
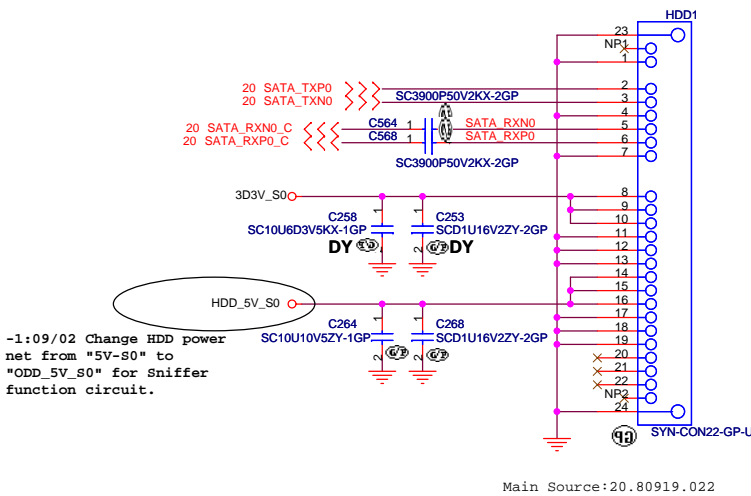
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

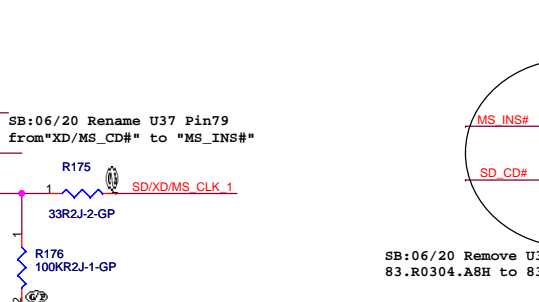
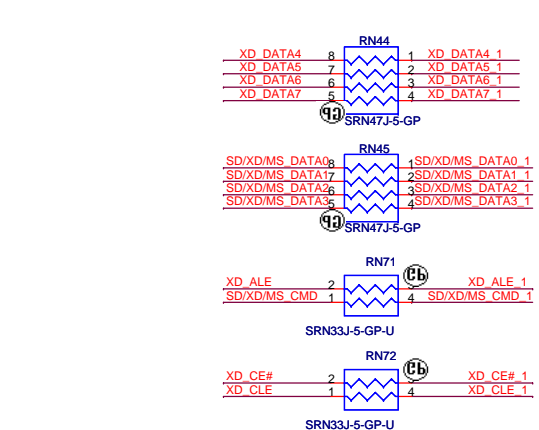
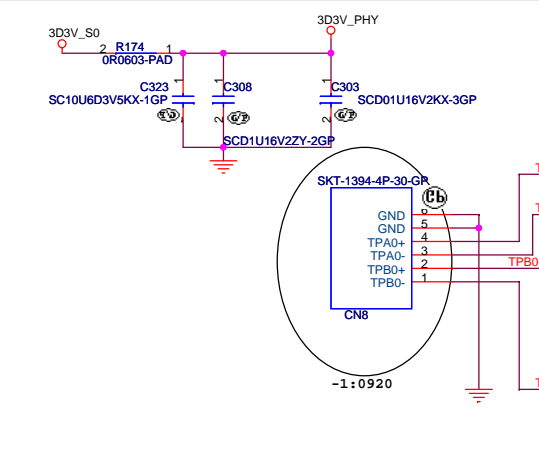
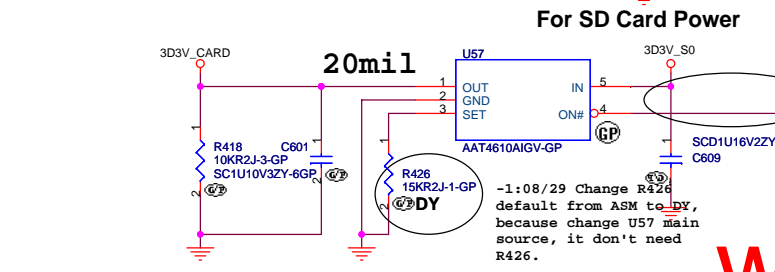
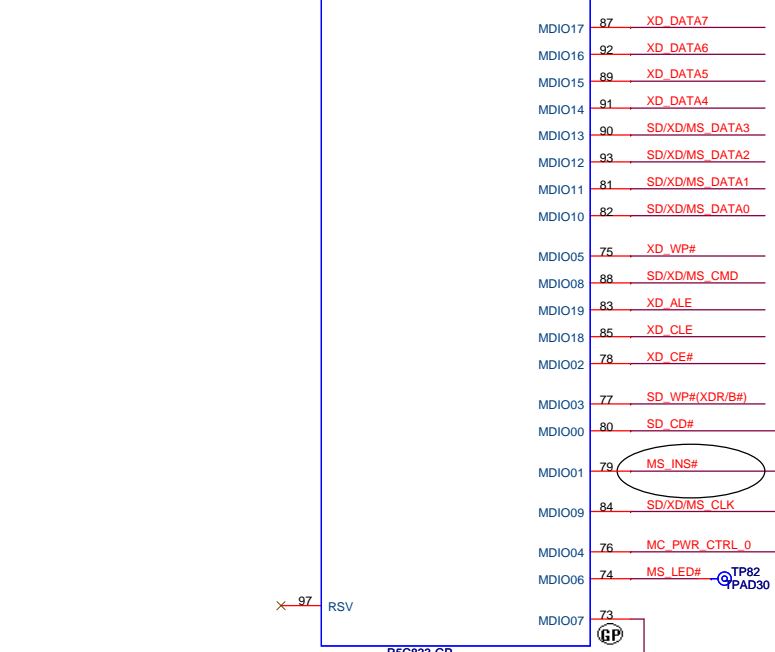
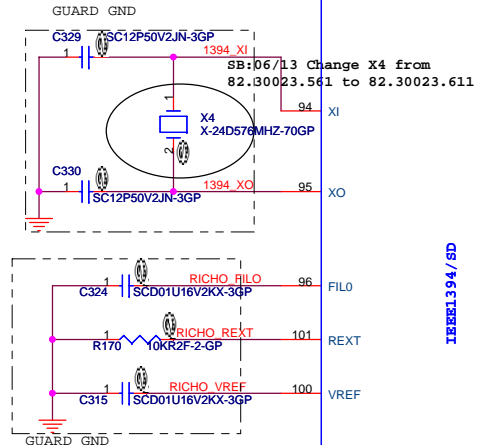
Title			
Sil 1392 HDMI			
Size A3	Document Number		Rev -3
DS2-Intel			
Date: Wednesday, January 23, 2008	Sheet 23	of 47	

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SATA HD Connector

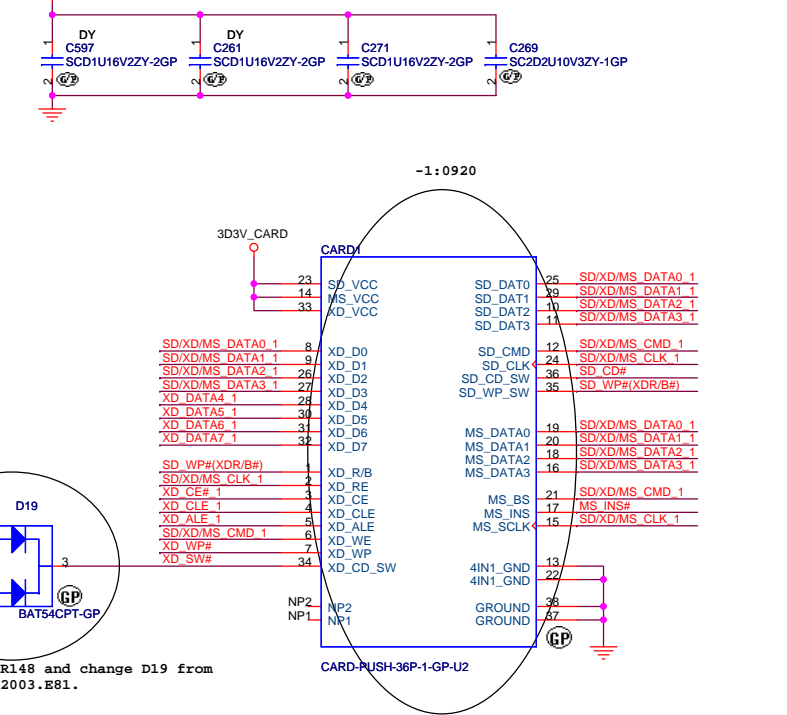
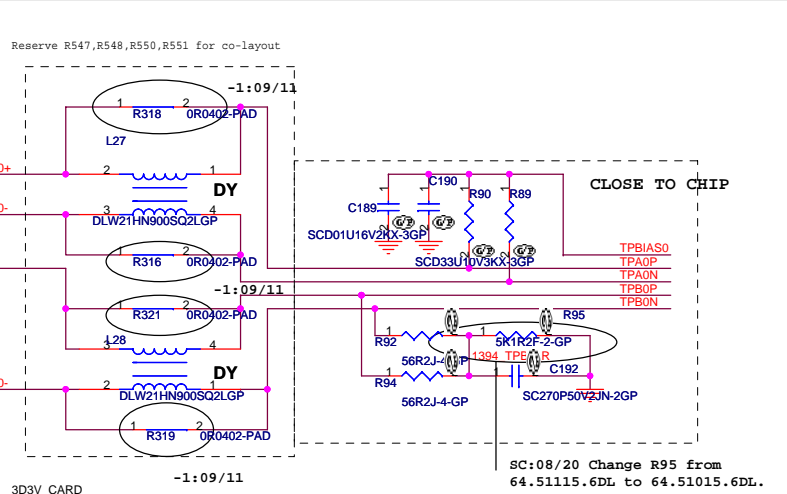
CD-ROM Connector





SB:06/20 Remove R427 and change U57 pin4 connect to "MC_PWR_CTRL_0"

Part	Value
RT9711DPBG	DY
G5240D2T1U	DY
AAT4610AIGV	15K

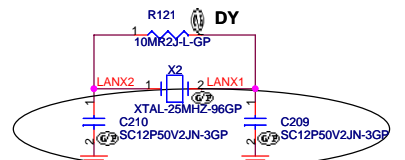


SB:06/20 Remove U35, R148 and change D19 from 83.R0304.A6H to 83.R2003.E81.

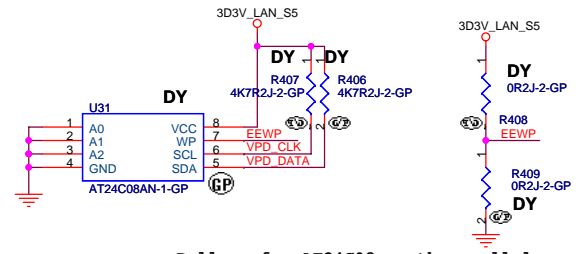
Part	Value
RT9711DPBG	DY
G5240D2T1U	DY
AAT4610AIGV	15K

	R394	R354	R357	R362	R372	R377	C528	C544
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

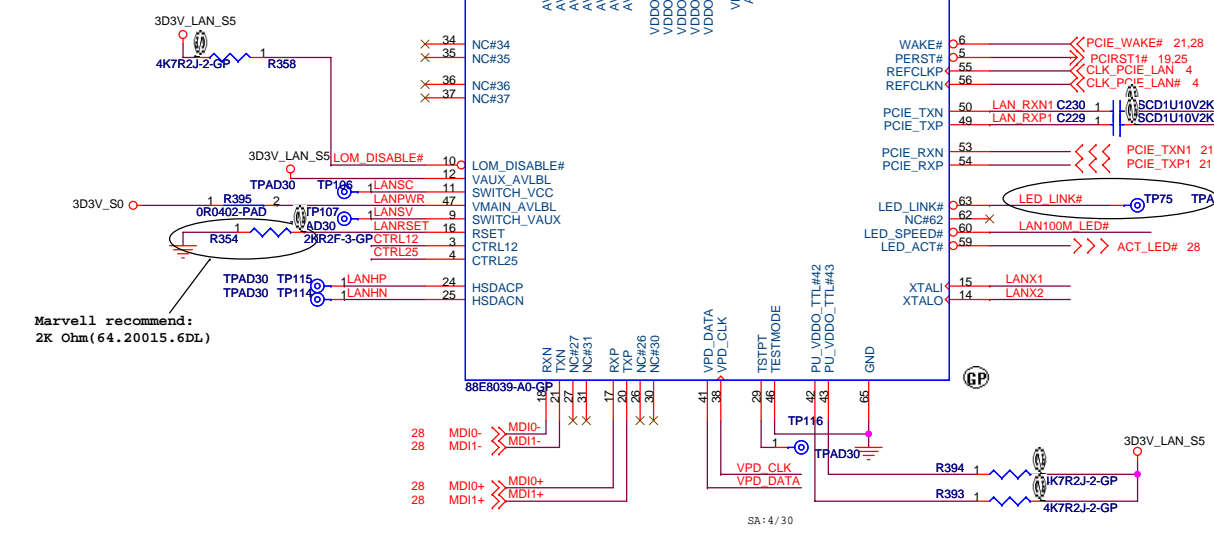
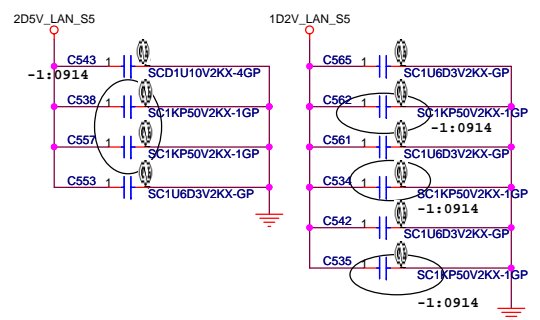
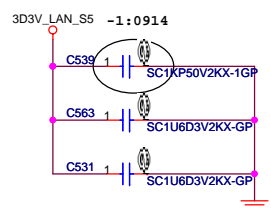
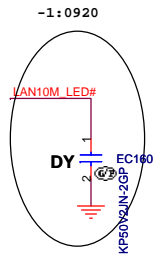
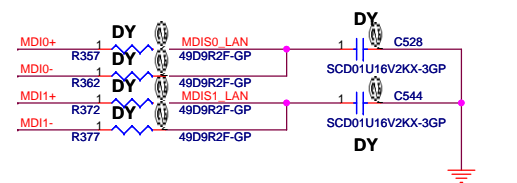
Note: Default is 88E8040



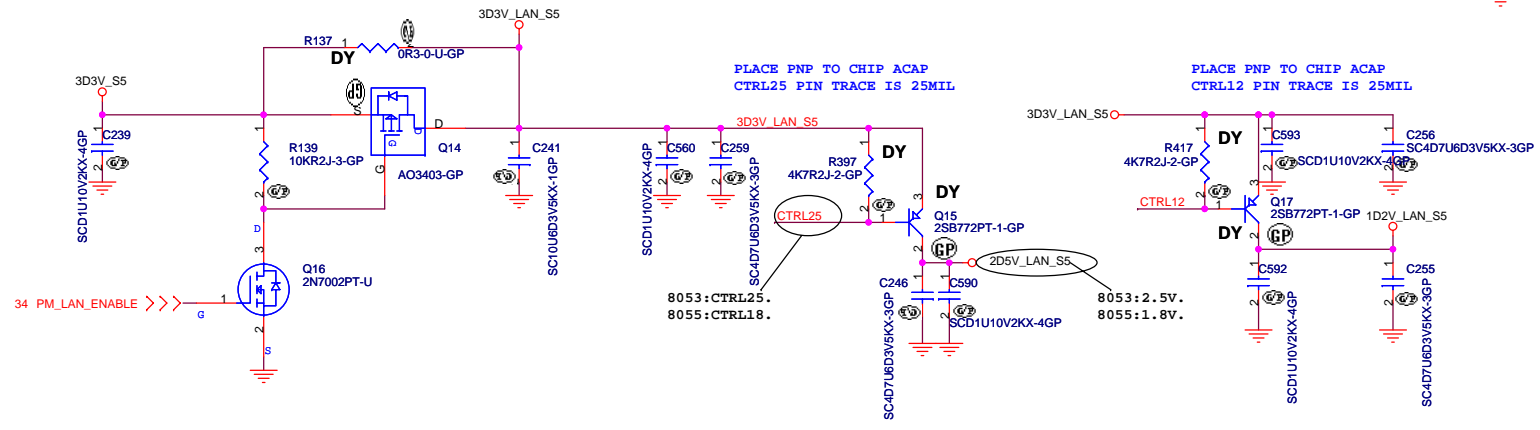
SB:06/13 Change C209,C210 from 27P to 12P



Pull up for AT24C08 another pull low



	R397	Q15	R417	Q17
88E8039	4K7	2SB772PT	4K7	2SB772PT
88E8040	DY	DY	DY	DY



<Core Design>

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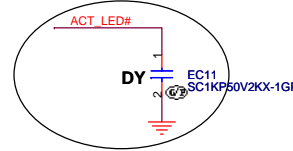
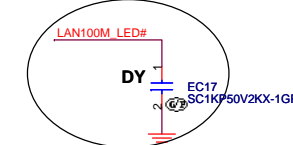
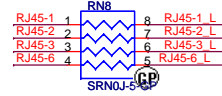
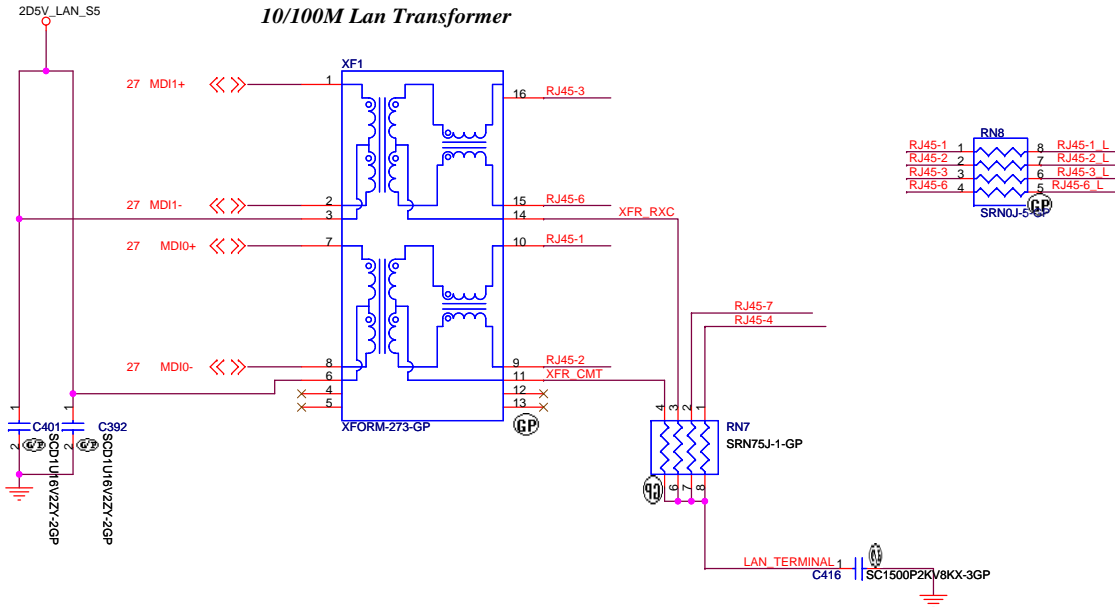
Title: **LAN MARVELL**

Size A3 Document Number: **DS2-Intel** Rev: **-3**

Date: Monday, January 21, 2008 Sheet 27 of 47

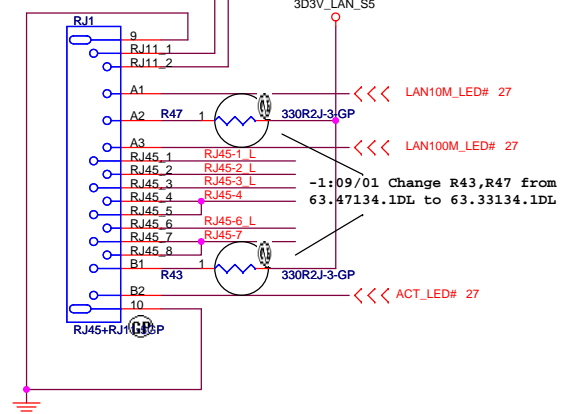
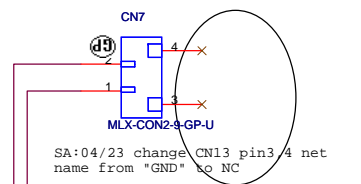
RJ45 Connector

10/100M Lan Transformer



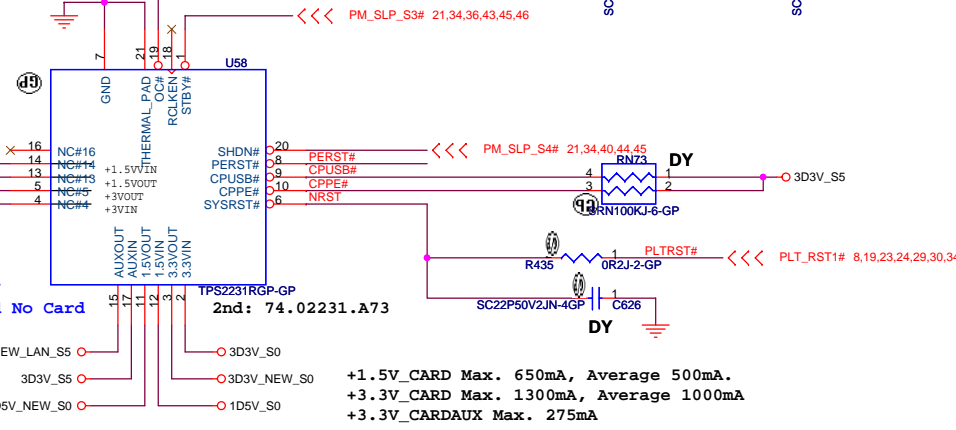
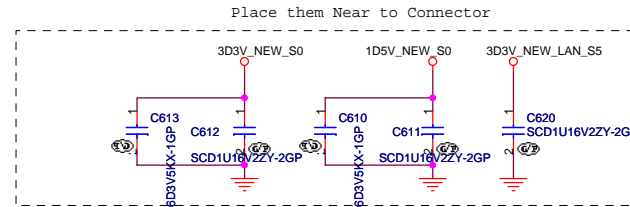
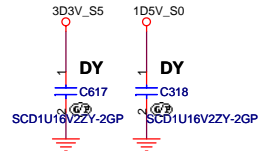
Green : Link up
Blinking : TX/RX activity

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



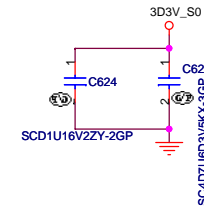
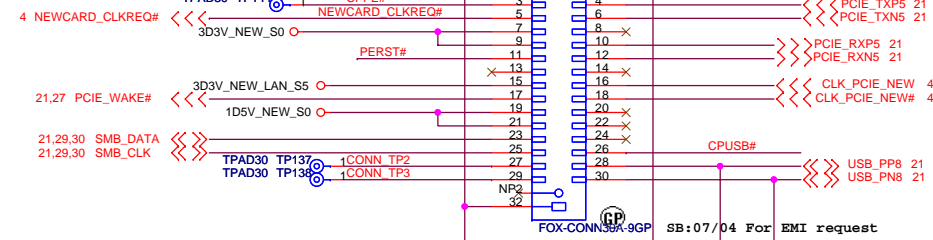
NEWCARD Connector

Place them Near to Chip



Test circuit
Use Card and No Card

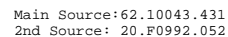
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



<Core Design>

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Title		
LAN connector/NEW CARD		
Size	Document Number	Rev
A3	DS2-Intel	-3
Date:	Monday, January 21, 2008	Sheet 28 of 47

SB:06/22 Change MINI1,2,3 slot from
62.10043.431 to 62.10043.551(only
modify properties)



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Title

11

Size

A3

Date: Monday, January 21, 2008

MINI CARD CONN 1**DS2-Intel**

Rev

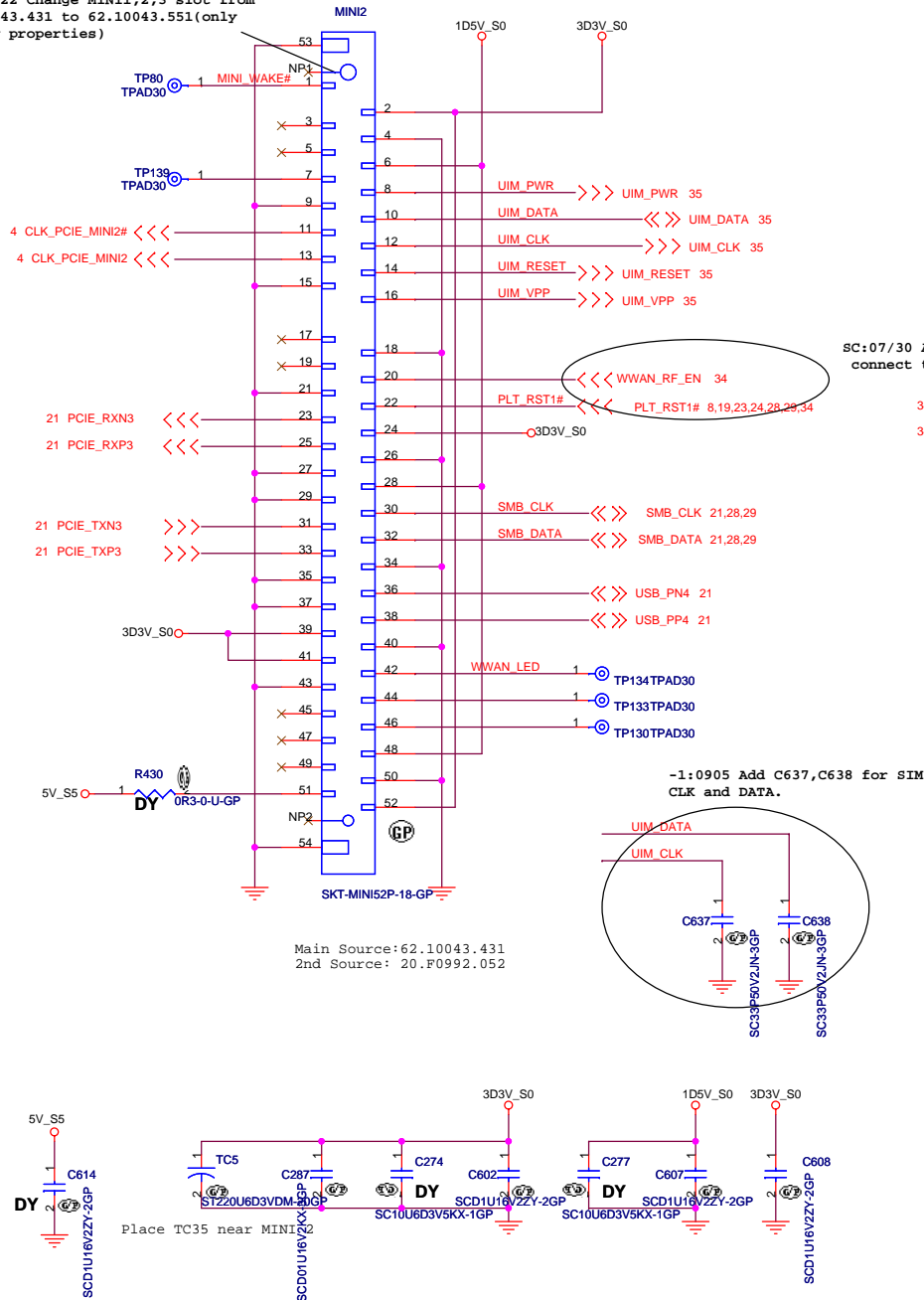
-3

47

Mini Card Connector

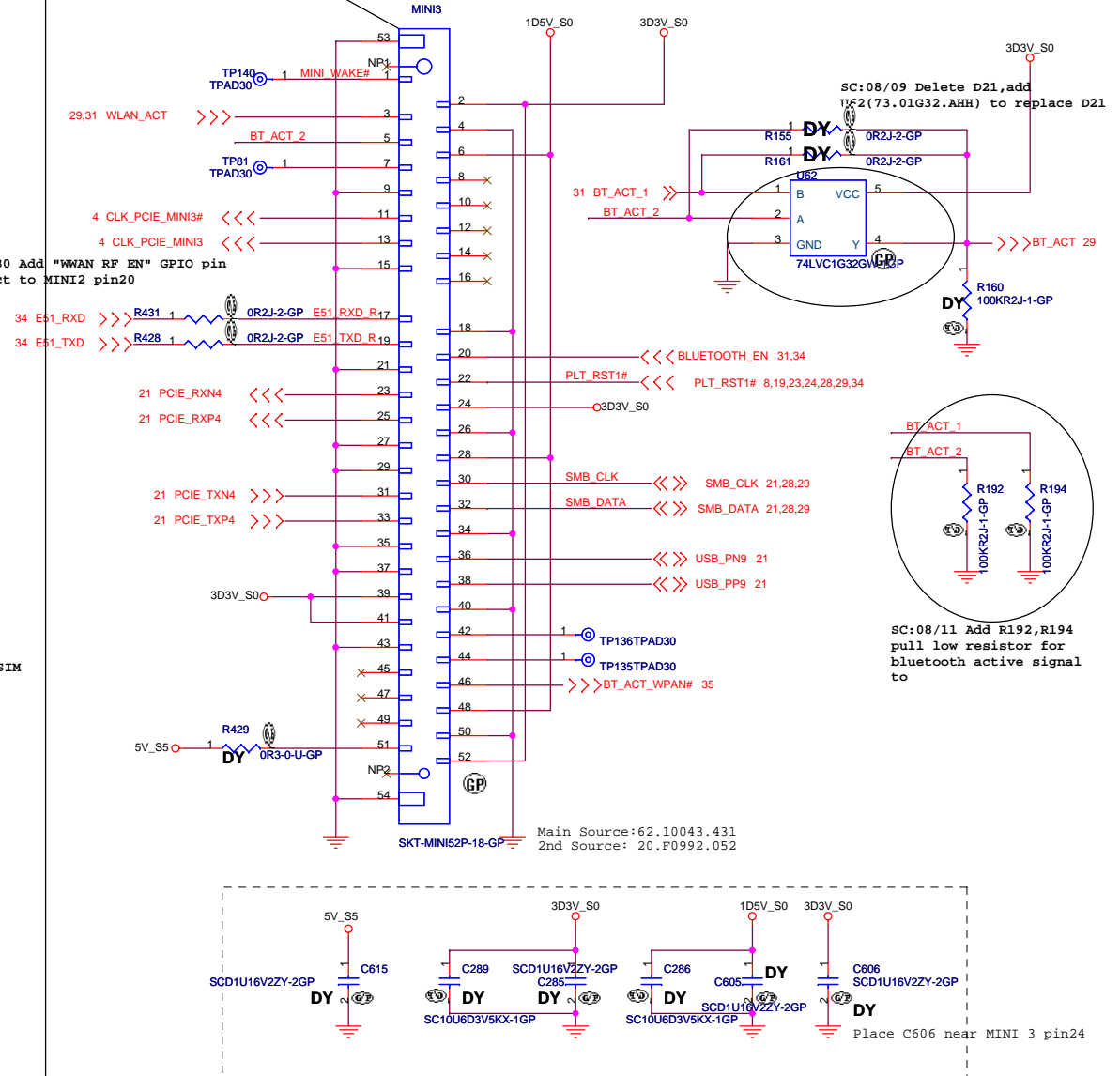
Mini Card Connector 2(WWAN)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)



Mini Card Connector 3(Robson)

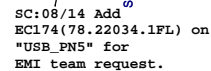
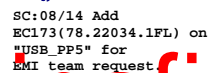
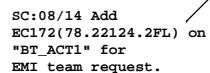
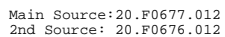
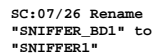
SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)

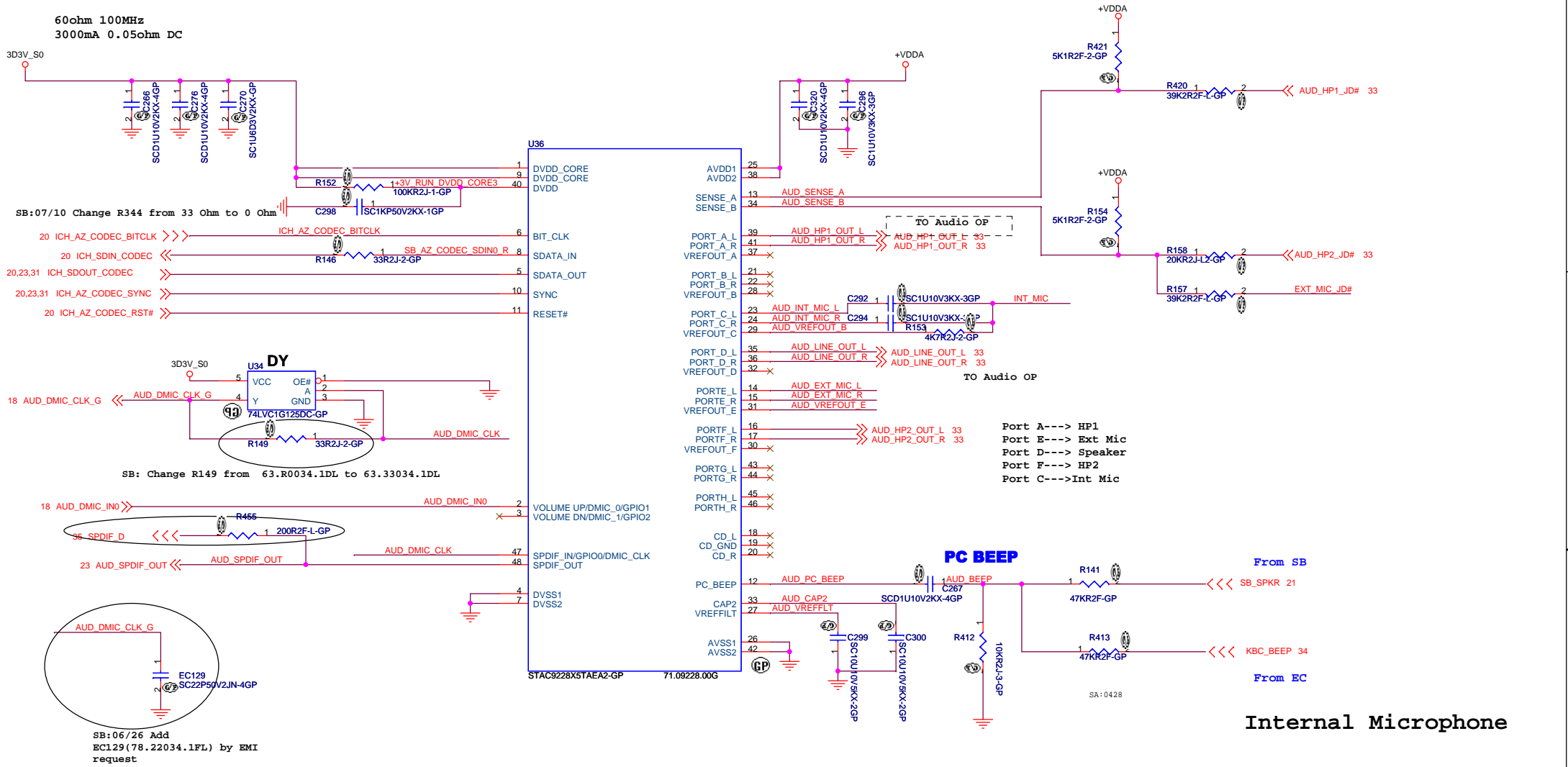


<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			MINI CARD CONN 2 & 3	
Size	Document Number	Rev		
A3	DS2-Intel	-3		
Date:	Wednesday, January 23, 2008	Sheet	30	of 47





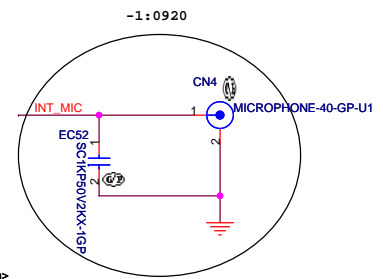
Internal Microphone

Azalia I/F EMI

Azalia I/F EMI

-1:0921 Remove R144 and C265

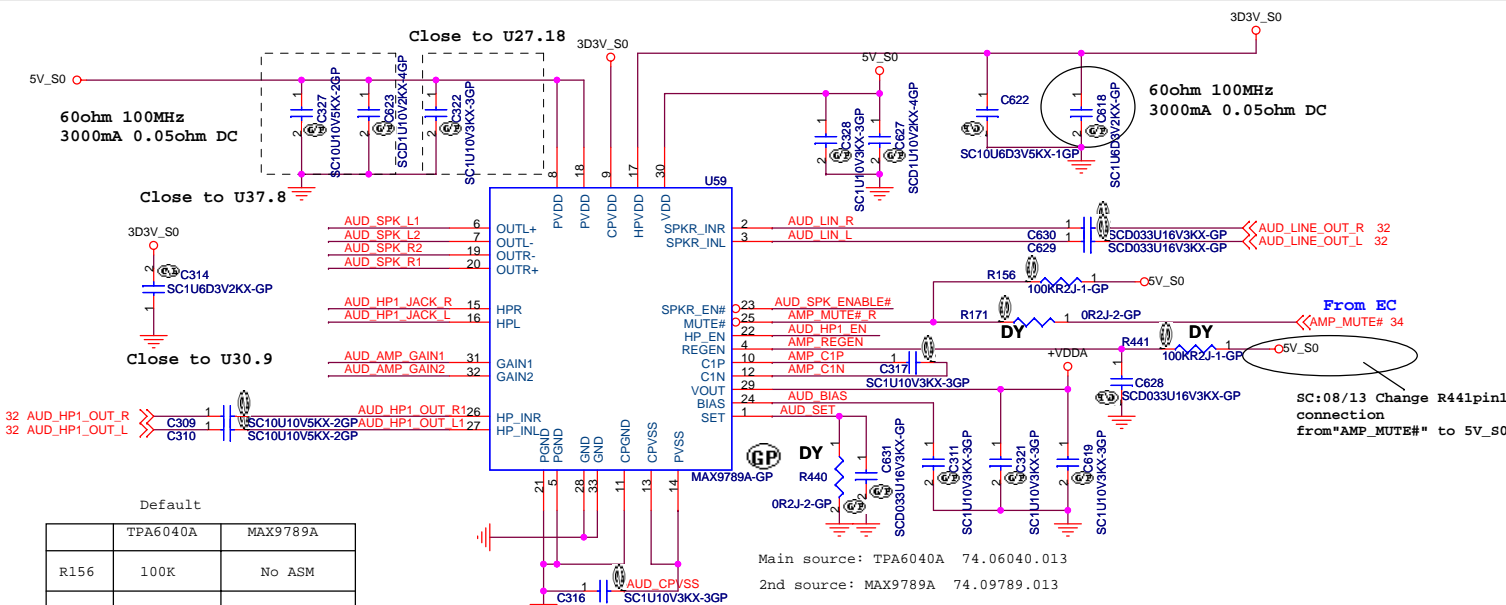
MIC IN



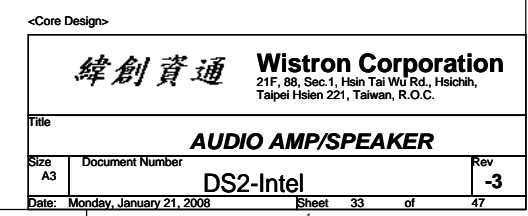
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Taipei Hsien 221, Taiwan, R.O.C.

Title			AUDIO CODEC STAC9228		
Size	Document Number	DS2-Intel			Rev
A3					-3
Date:	Monday, January 21, 2008	Sheet	32	of	47



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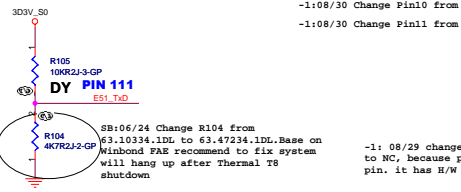


WPC8763L STRAP PIN

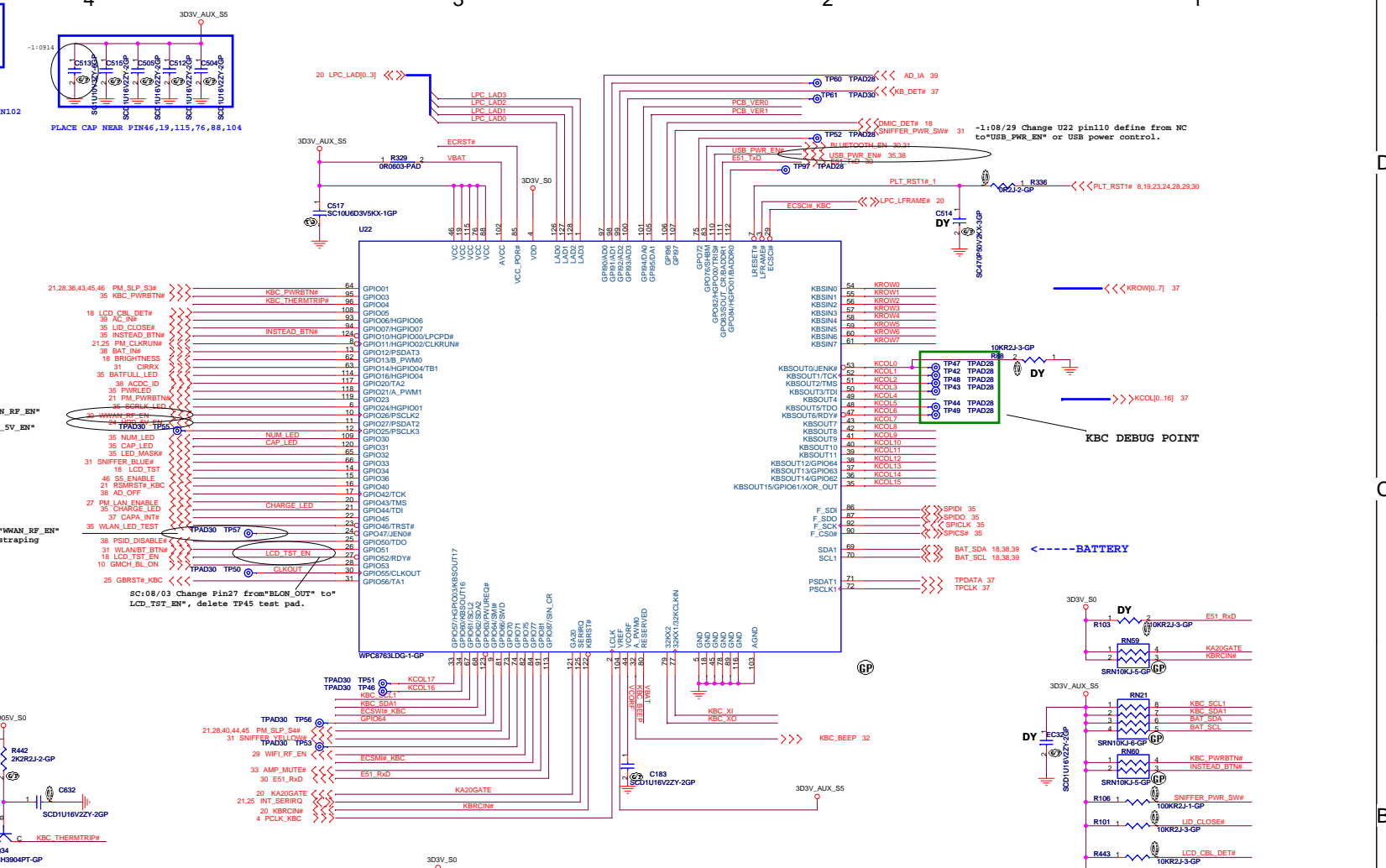
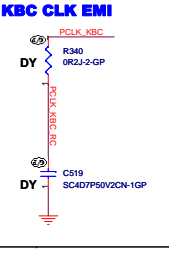
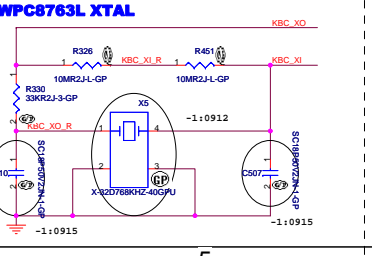
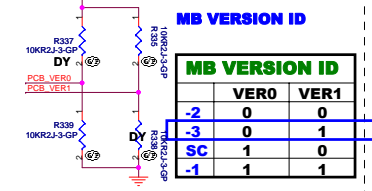
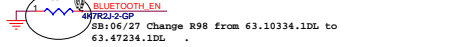
JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	NO PD	GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE
Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is connected.

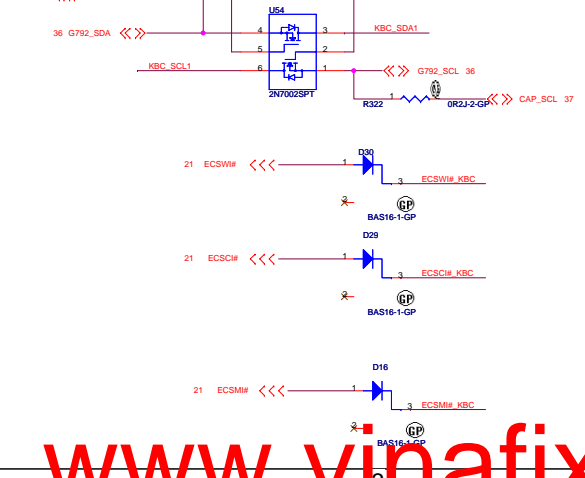
BADDR1-0 (PIN 111, 112) I/O Base Address.
10KΩ external pull-down resistor on BADDR1: Core defined



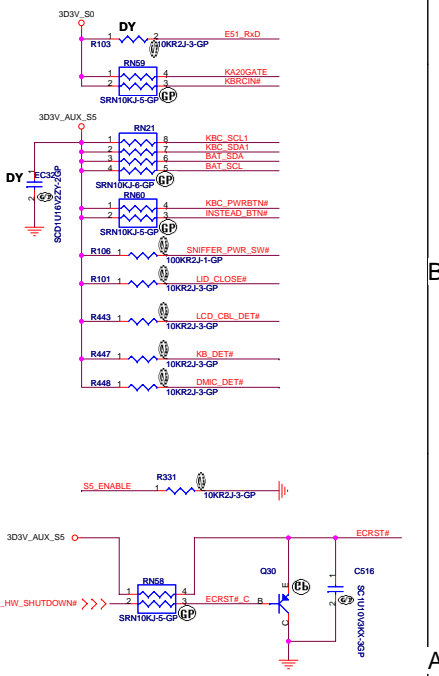
SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.

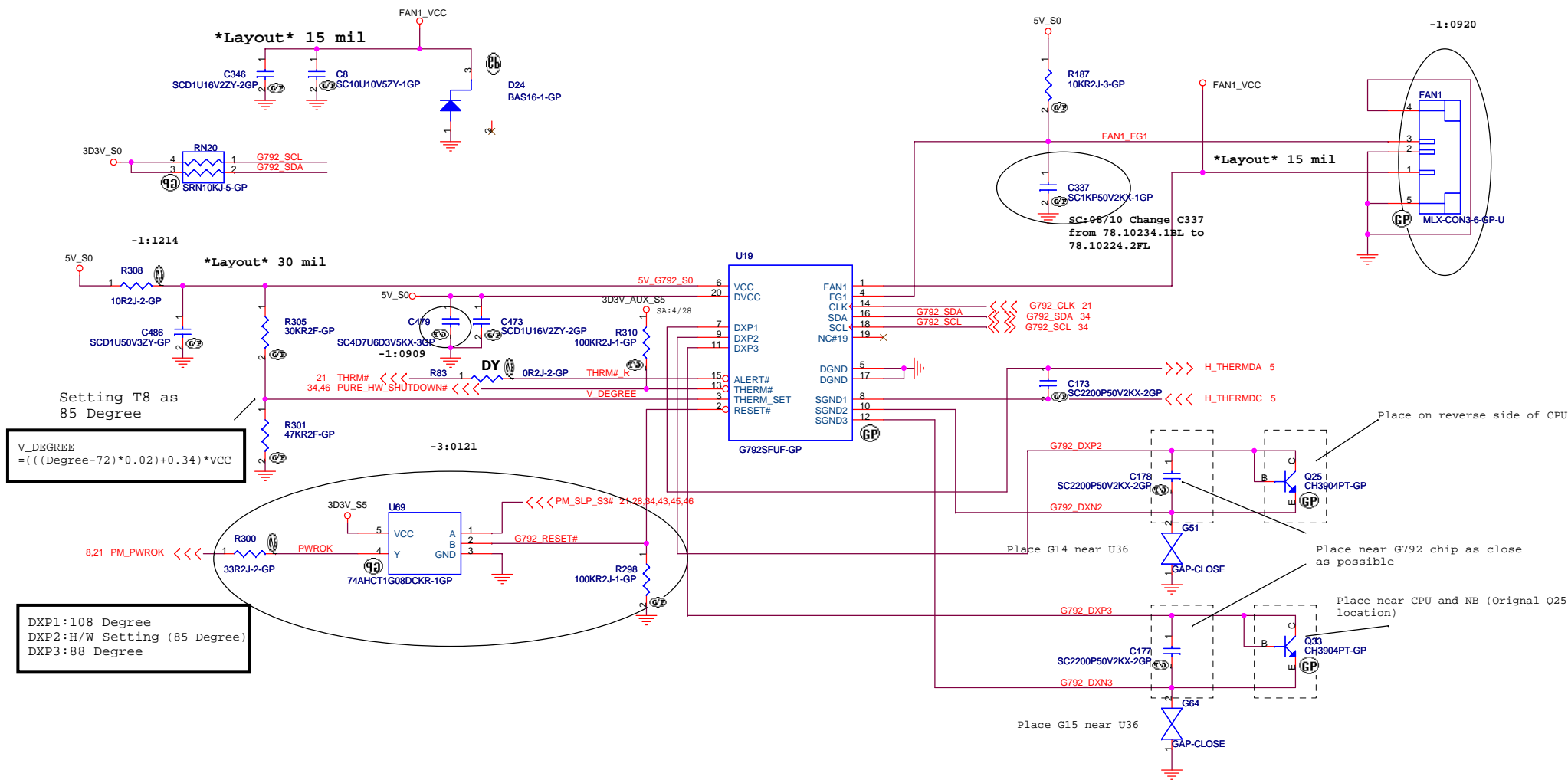


FOR Thermal AND Capacity Button Module



ADIA:to Charger
ACDC_ID:from Adapter Conn
KBC_PWRBTN#:from power button
BAT_IN#:from Battery Conn
DC_BATFULL#:for Battery charge LED 1
WLAN_TEST#:for WKS test WLAN LED
AD_OFF:enable AC adapter power source
CHARGE_LED#:for Battery charge LED 2
WLAN_BT_BTN#:from Wlan on/off button
GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip
WIRELESS_EN:Disable/Enable Wireless Module
BLUETOOTH_EN:Disable/Enable Bluetooth
USB_PWR_EN#:to on/off USB power switch
CCD_ON:Webcam power on/off
AC_IN#:From Charge



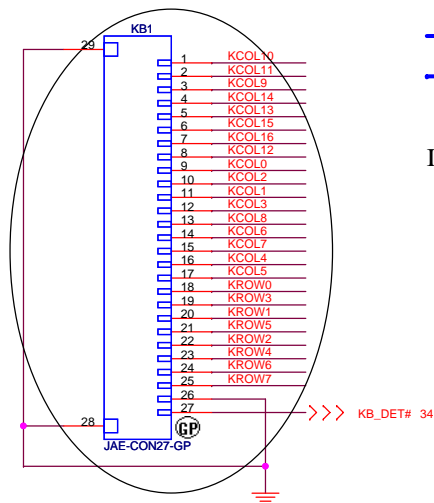


<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

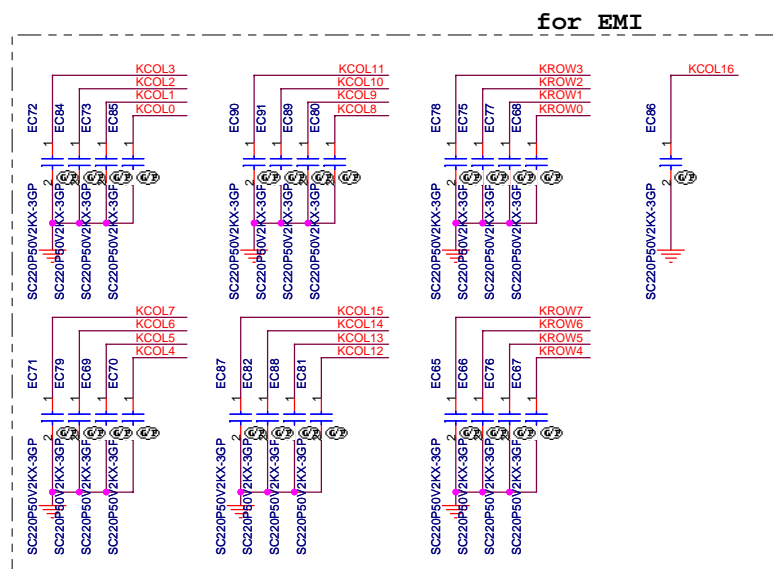
Title		
Thermal/Fan Controller G792		
Size	Document Number	Rev
A3	DS2-Intel	-3
Date:	Wednesday, January 23, 2008	Sheet 36 of 47

SB:06/27 Change K/B connector from 20.F0694.025 to 20.K0291.027 .

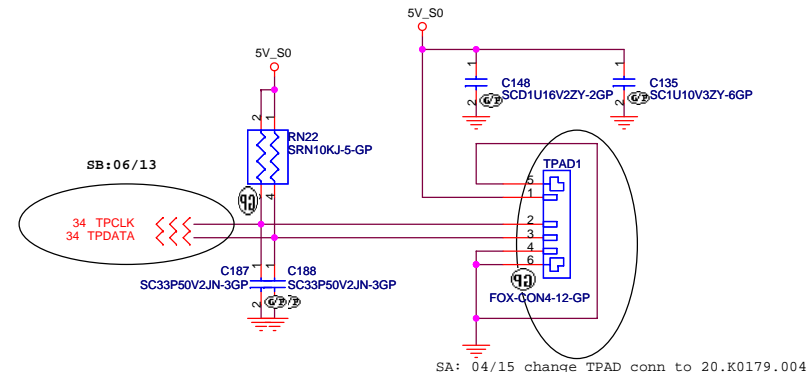


<<< KROW[0..7] 34
 >>> KCOL[0..16] 34

Internal KeyBoard Connector

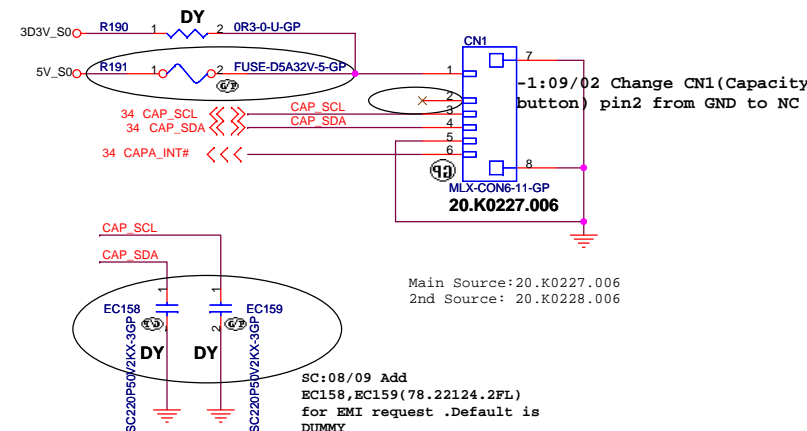


TouchPad Connector



-1:12/14 Chage R191 from 0 ohm to 0.5A fuse to prevent VCC short to GND.

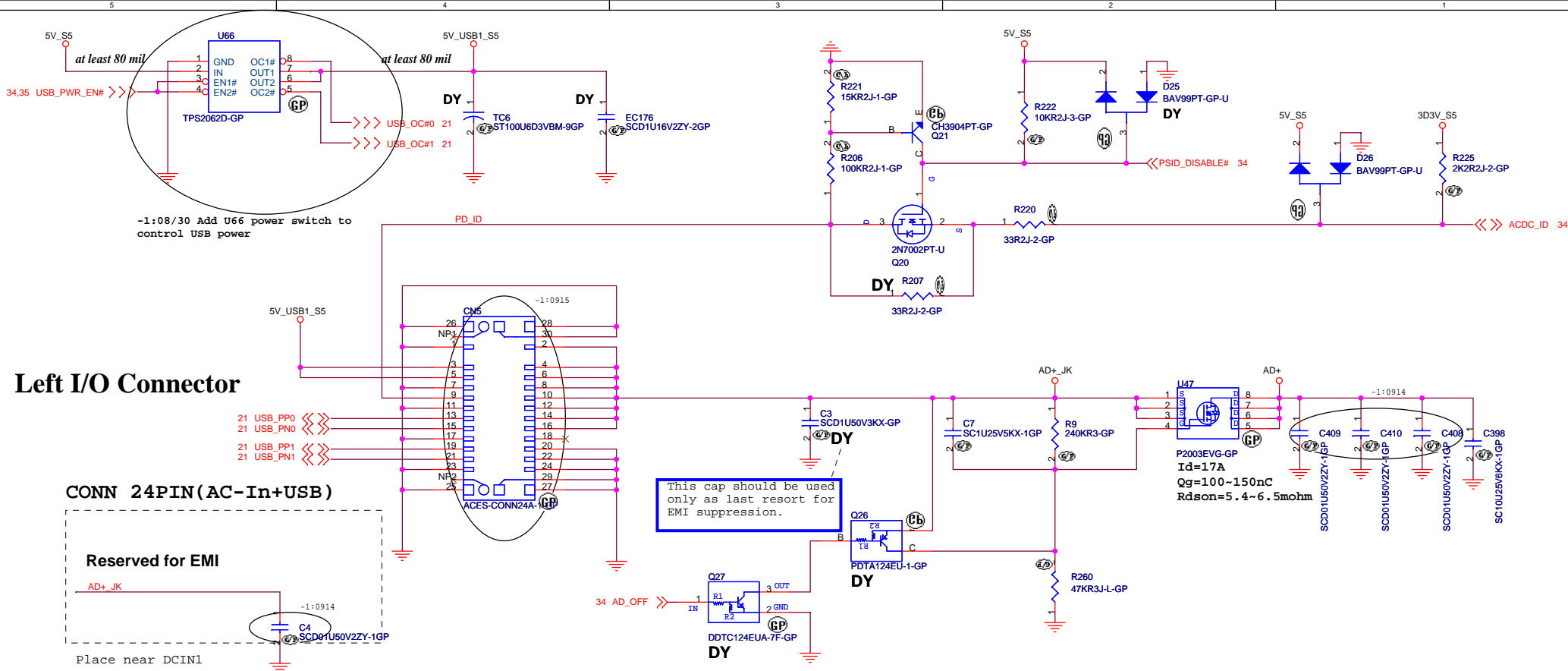
CAPACITY BUTTON

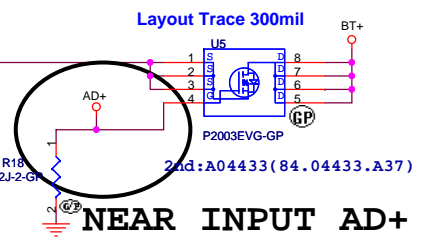
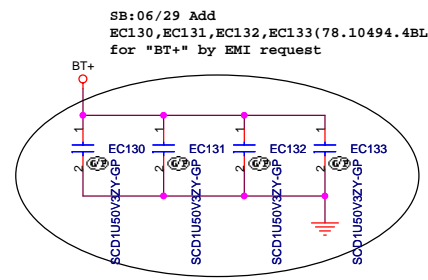
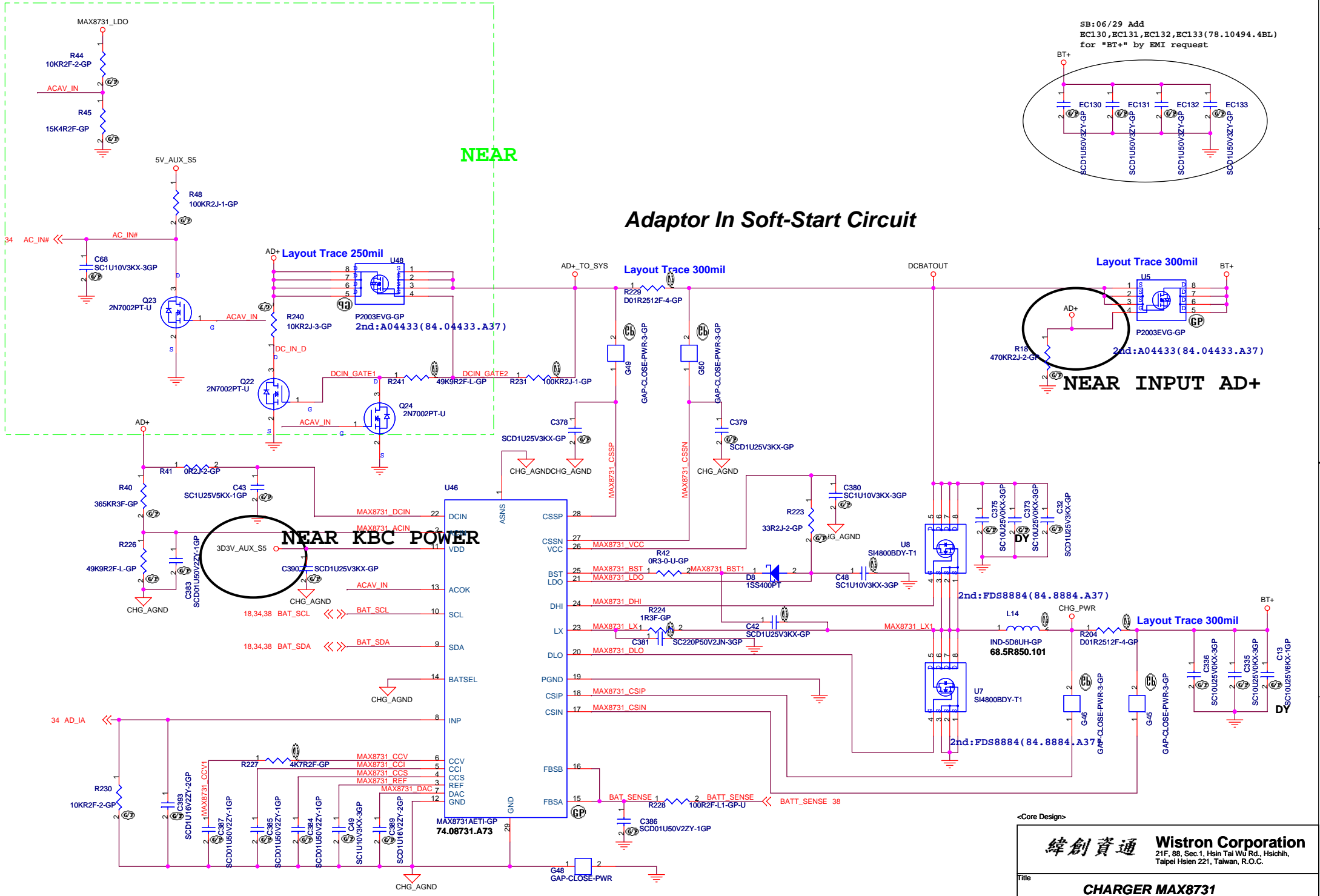


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Title		
KeyBoard-CONN		
Size A3	Document Number	Rev
	DS2-Intel	-3
Date: Monday, January 21, 2008	Sheet 37 of 47	

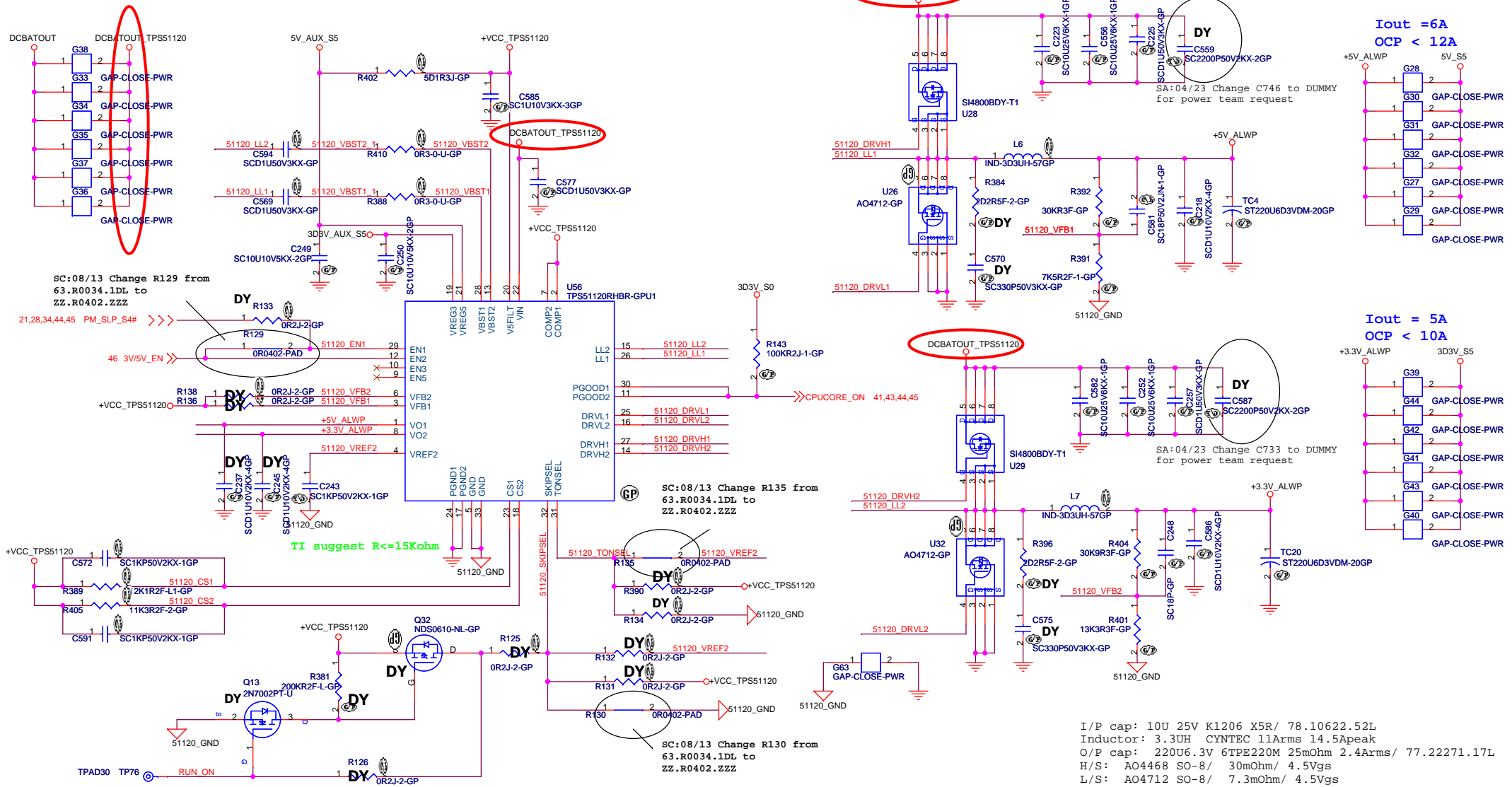




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File: **CHARGER MAX8731**

Size A3	Document Number DS2-Intel	Rev -3
Date: Monday, January 21, 2008	Sheet 39 of 47	



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Taipei Hsien 221, Taiwan, R.O.C.

Title			DC to DC 3.3V & 5V		
Size	Document Number		DS2-Intel		Rev
A3					-3
Date:	Monday, January 21, 2008		Sheet	40	of 47

SB:06/17 Remove R205,C348,TP86 power monitor circuit.

Place close to phase 1 choke
5 CPU_PROCHOT#
470K /0402 size
If NTC=330Kohm, R10=8.66K

6 CPU_VID[0..6]

SC:08/13 Change R28 from 63.00000.00L to ZZ.R0603.ZZZ

SC:08/13 Change R27 from 63.00000.00L to ZZ.R0603.ZZZ

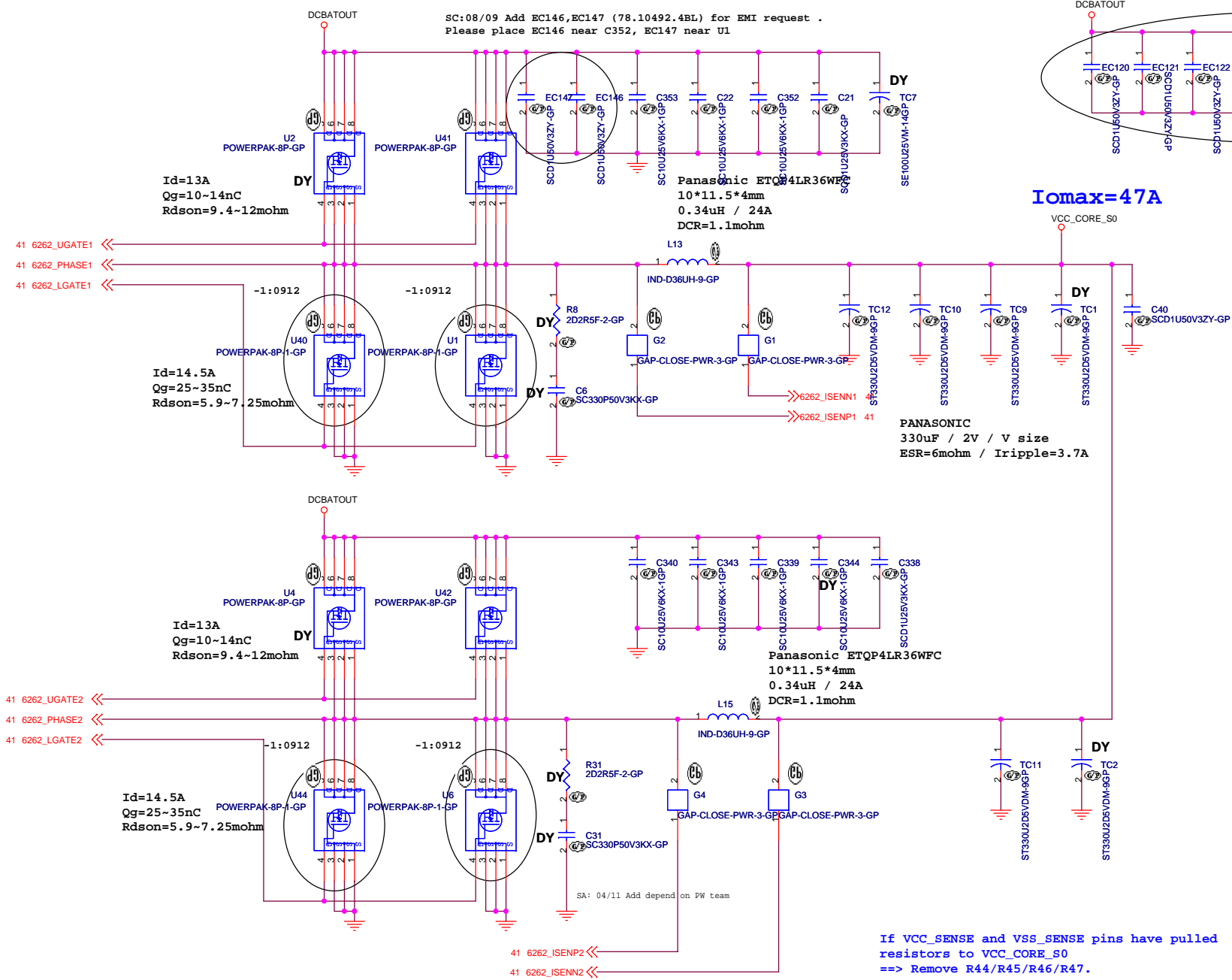
When test without cpu,
R483 & R486 change to 0 ohms

Place close to phase 1 choke

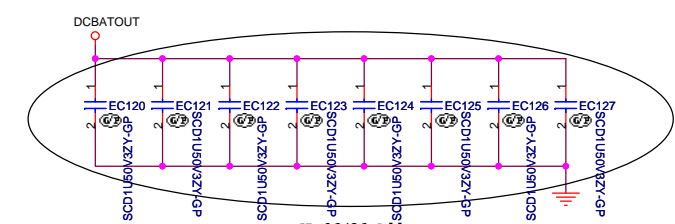
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Title			DC-DC VCCCPUCORE 1/2
Size	Document Number	Rev	
A3	DS2-Intel	-3	
Date:	Monday, January 21, 2008	Sheet	41 of 47



Iomax=47A

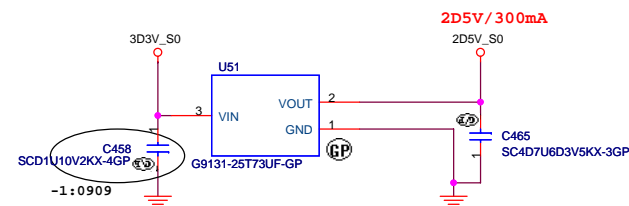
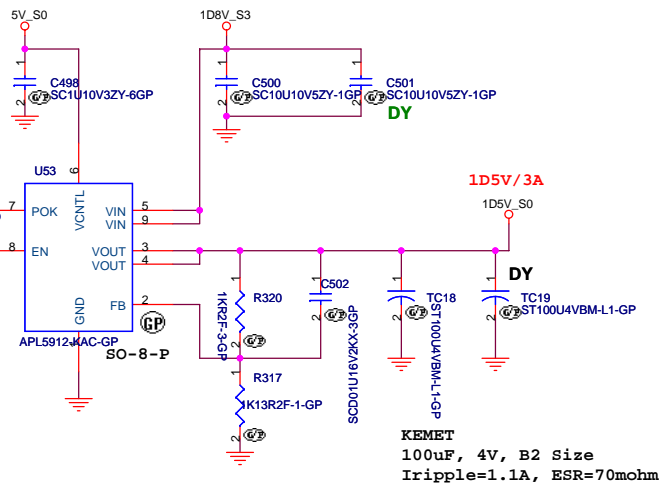


1D5V_SB

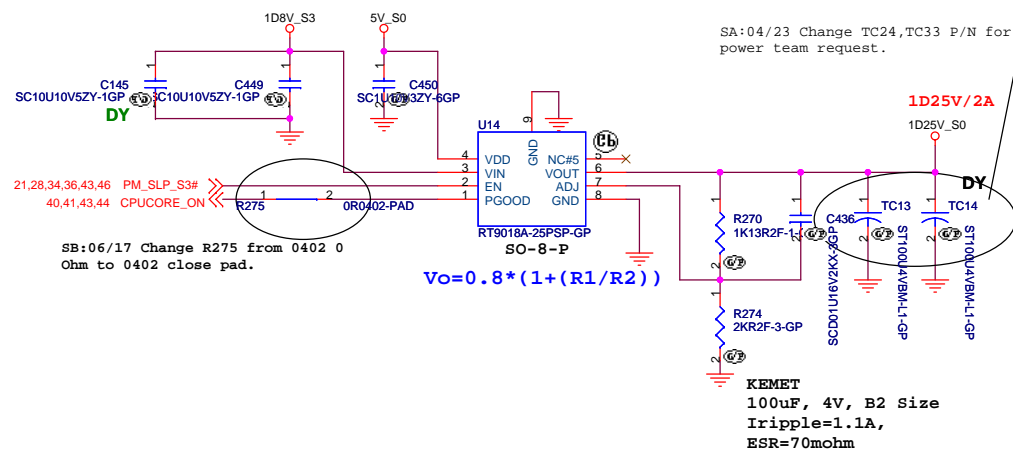
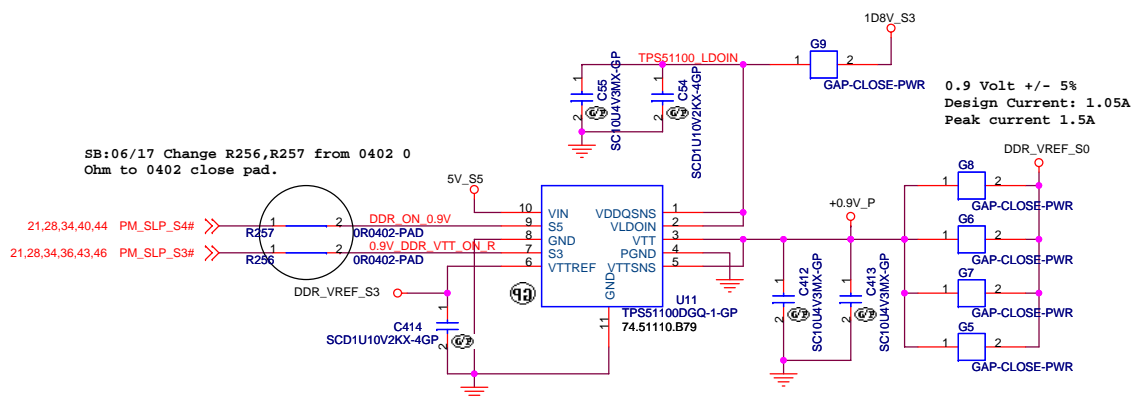
SB:06/17 Change R315 from 0402 0
Ohm to 0402 close pad.

40,41,43,44 CPUCORE_ON << R315

$$V_o = 0.8 * (1 + (R_1/R_2))$$



```
SSID = PWR.Plane.Regulator_0.9V
```



<Variant Name>

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Title

DC/DC 1D8V

Size

Document Number

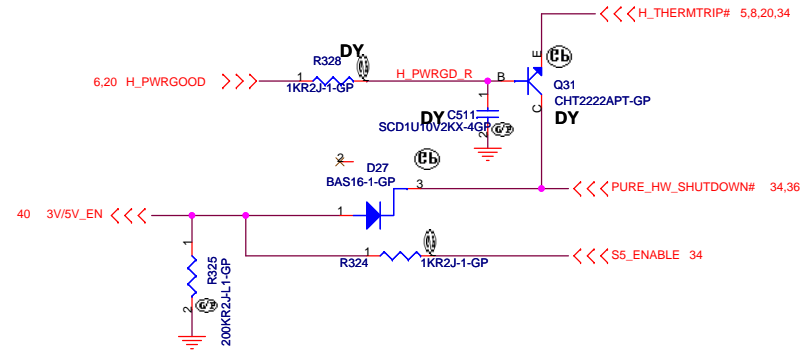
DS2-Intel

Rev

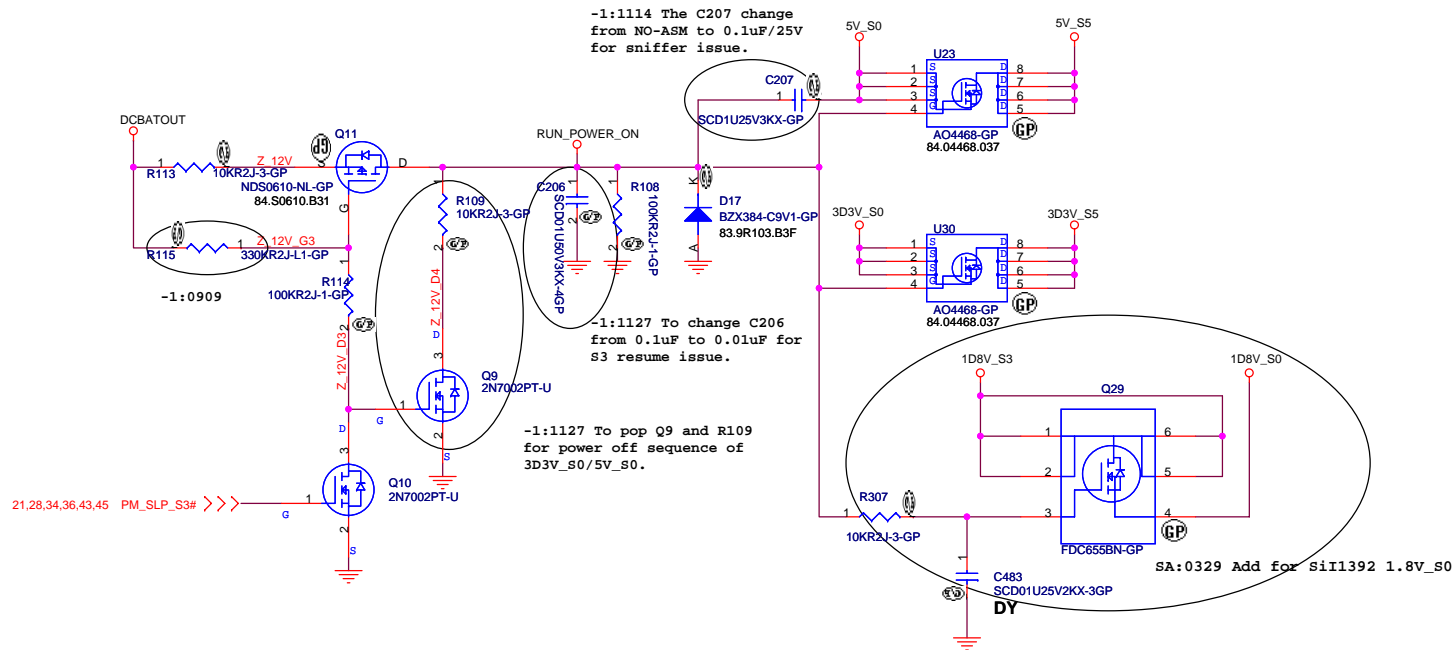
Date: Monday, January 21, 2008

Sheet 45 of

47



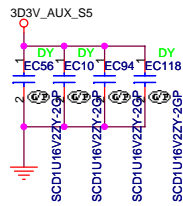
Run Power



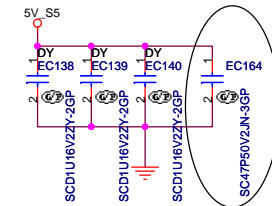
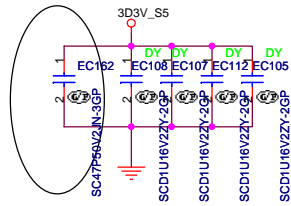
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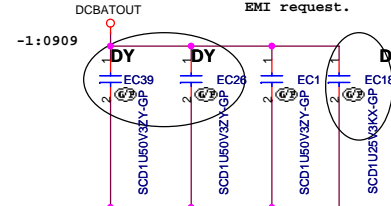
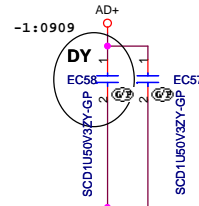
Title			PWRPLANE&RESETLOGIC	
Size	Document Number	DS2-Intel		Rev
A3				-3
Date:	Monday, January 21, 2008	Sheet	46	of 47



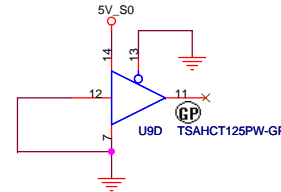
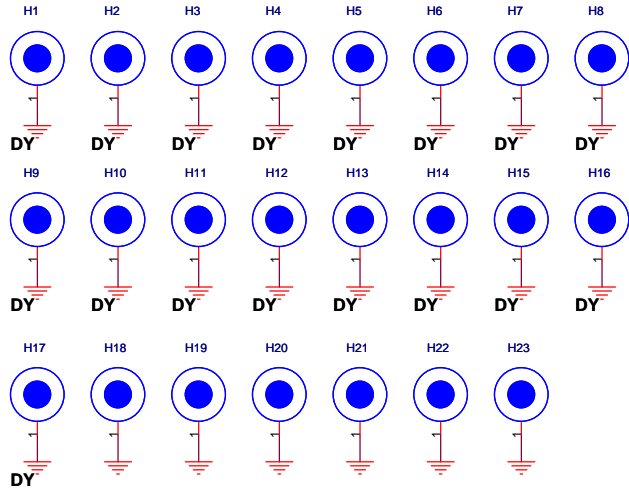
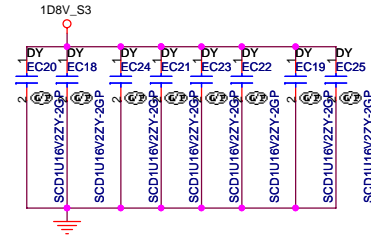
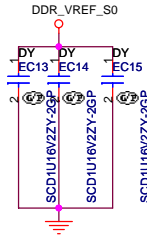
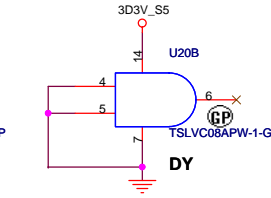
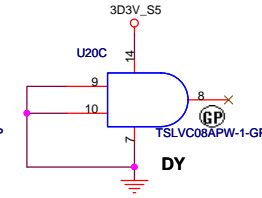
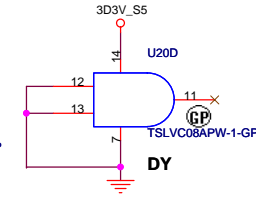
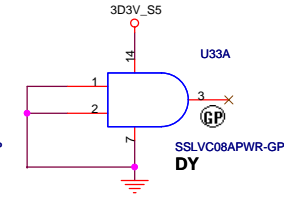
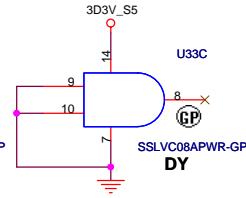
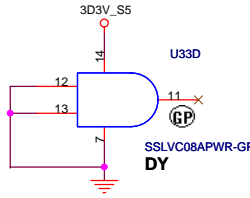
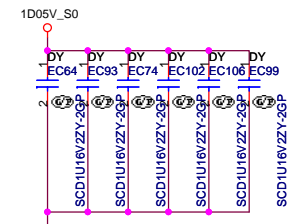
SC:08/11 Add EC162 on 3D3V_S5 for RF team Request.



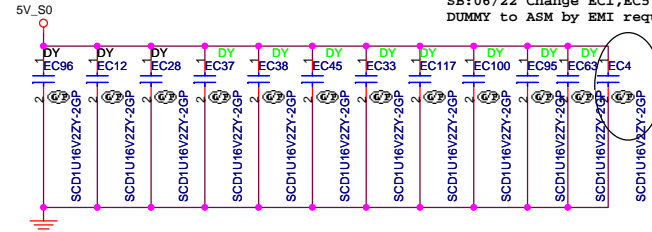
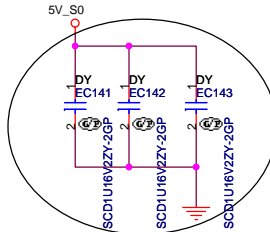
SC:08/11 Add EC164 on 5V_S5 for RF team Request.



-1:0904 Add EC187(78.10422.2BL) for DCBATOUT decoupling, this is for EMI request.

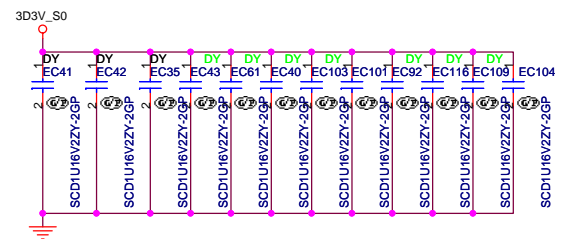
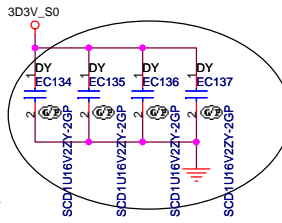


SB:06/29 Add EC141, EC142, EC143(78.10491.4FL) for EMI request

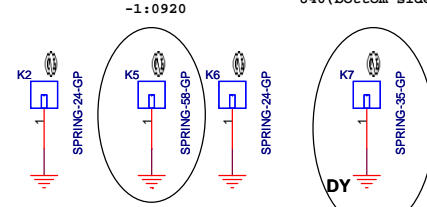
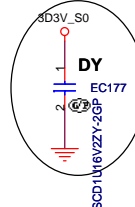


SB:06/22 Change EC1, EC5 from DUMMY to ASM by EMI request.

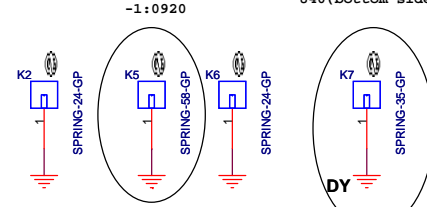
SB:06/29 Add EC134, EC135, EC136, EC137(78.10491.4FL) for EMI request



SC:08/15 Add EC177(78.10491.4FL) on 3D3V_S0, this is for EMI request. Default is DY



Place this spring near U40(bottom side)



SC:08/11 Change K7 from 34.39S07.001 to 34.41P18.001.This change is for EMI request
-1:11/15 Remove K7 for no used.

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Title		
MISC		
Size A3	Document Number	Rev
	DS2-Intel	-3
Date: Monday, January 21, 2008	Sheet 47 of 47	